IMEC demonstrates viability of laser anneal for the 32nm node

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At today's IEEE International Electron Devices Meeting, IMEC reports that laser anneal is a promising option for further transistor scaling to the 32nm node. By device demonstration, IMEC shows that laser anneal allows to scale junction depth without degradation of series resistance and overlap capacitance.

Sub-melt laser anneal stands out as a promising option to allow further transistor scaling by improving the gate depletion effects and consequently delaying the need to introduce metal gate process alternatives at 45nm. Up to now, the use of laser anneal has been hampered by the impact of the steep thermal gradients on the dielectric resulting in high mechanical stress and consequently reduced transistor lifetime.

By optimizing the dielectric integrity and laser anneal conditions, IMEC demonstrates that optimal performance and transistor lifetime can be achieved with no loss of dies near wafer edge. Laser anneal results in improved transistor performance by a significant reduction of the minimum sustainable gate length, of the source-drain resistance and of the overlap capacitance.

In a first step, laser anneal was added to the conventional spike anneal achieving good results for the 45nm node. The combination of spike and laser anneal enabled a reduction of the minimum gate length by 15nm for nMOS and by 5nm for pMOS compared to standard poly-Si/SiON. The overlap capacitance was improved with 8% and the source-drain resistance was reduced with 10%.

The full potential of laser anneal as the sole thermal process to activate dopants was demonstrated on devices with metal gate electrodes. A minimum gate length gain of 25nm for nMOS and of 20nm for pMOS devices was achieved compared to devices made with a conventional spike anneal process. The overlap capacitance of only 0.26fF/µm for both nMOS and pMOS was nearly optimal for implementation. A performance gain of 8% was achieved for pMOS due to a 25% lower source-drain resistance. Thanks to the reduced overlap capacitance for both nMOS and pMOS and the increased performance of pMOS, the intrinsic delay was lowered with 18% for nMOS and 23% for pMOS.

These results were obtained in close collaboration with Applied Materials and within IMEC's core program on (sub-)32nm CMOS, which joins forces from nine of the world's leading IC manufacturers or foundries (Infineon, Intel, Micron, NXP, Panasonic, Samsung, STMicroelectronics, Texas Instruments and TSMC).

Source: IMEC

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