Philips introduces Advanced Ultra-low Power CMOS logic family in industry's smallest package

19 September 2005

Royal Philips Electronics today introduced its family of Advanced Ultra-low Power (AUP) CMOS logic, featuring ultra-low power consumption. The AUP logic family offers more than 55 new products available in two package options, PicoGate and MicroPak. The AUP family offers the lowest power consumption available in a logic device, offering a 30 percent advantage over other families. This allows for extended battery life in devices such as cell phones, PDAs, digital still cameras and video players.

The electronics industry is moving toward more sophisticated electronic devices in increasingly smaller packages that require less power. The innovations inherent in the AUP family address these needs and make it easier for manufactures to design new applications for the home, personal, automotive and mobile markets. According to a recent market forecast published by industry research firm Insight Onsite, the 1.8V logic product market is expected to grow over 53 percent from 2006 to 2008 – from 223 million in 2006 to 343 million in 2008 – making this an ideal time for Philips to introduce the new AUP logic family.

"Forecasts show that the consumer electronics market will generate annual revenue in excess of US$38 billion by 2009, and the AUP market alone is expected to have a 27 percent compound annual growth rate from 2005 to 2009," said Bruce Potvin, director of marketing, Logic Products Group at Philips Semiconductors. "Given these growth rates, it’s easy to see why Philips is dedicated to bringing new advanced logic solutions to our customers so they can have the parts they need to easily develop compelling new products for the consumer electronics market."

The AUP logic family comprises single, dual and triple gate functions housed in a 5-,6-, and 8-pin packaging allowing engineers to select the exact functions they require. Additionally, translation functions enable designers to easily interface between different voltage systems The AUP family also uses the newest MicroPak technology from Philips, which allows for migration from 0.50mm lead spacing to 0.35mm lead spacing, with the full release expected to take place by Q1 2006. Furthermore, the AUP family provides higher Electrostatic Discharge (ESD) protection, making the logic devices less vulnerable to static electricity. Typical specifications for the AUP logic family are: operating voltage range 0.8V – 3.6V, propagation delays of 2.5n @ 2.5V and a Cpd = 4 pF or less.