IMEC concludes FEOL installation and enters into alliances for copper/low-k interconnect technology

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IMEC successfully concludes installation of front-end-of-line (FEOL) tools with processing of first pathfinder lots. Strategic agreements with leading equipment manufacturers Applied Materials, Inc., ASM International and LAM Research Corporation have been extended to ramp up equipment installation for copper/low-k interconnect technology during the second half of 2005.

IMEC completed the installation of the full set of front-end-of-line (FEOL) tools for 300mm wafer processing and proved the facility is up and running with first pathfinder lots. The facility covers all advanced processes up to silicide level for both IMEC's planar bulk CMOS and multi-gate (MuGFET, FinFET) devices. To realize this, strategic alliances were concluded in 2004 with more than ten of the world's leading equipment suppliers - AIXTRON AG, Applied Materials, Inc., ASM International, ASM-Lithography, Axcelis, Dainippon Screen Mfg. Co., Ltd. (DNS), FEI Company, KLA-Tencor, Lam Research Corporation, Tokyo Electron Limited (TEL) and SEZ.

The first pathfinder lots include bulk-Si nFET (targeting 45nm node) and SOI FinFET (targeting 32nm node) lots to demonstrate the readiness for moving the materials-and-device research projects from the 200mm to the new 300mm fab. The lithography of all critical levels is performed on the ASML /1250i immersion scanner. All lots have devices with physical gate length down to 40nm.TaN and TiN metal gates are used in combination with high-k dielectrics such as HfO2 for the gate stacks.

Installation of the copper/low-k interconnect technology tools will start in the second half of 2005. The agreements with Applied Materials, Inc., ASM International and LAM Research Corporation have been expanded towards interconnect technology which will enable IMEC and its partners to investigate the most advanced low-k and copper plating solutions for the sub-45nm technology node.

With the new 300 mm state-of-the-art copper/low-k infrastructure, IMEC's interconnect program will focus on integrating next-generation low-k dielectrics for the 32nm node. Deposition and post-deposition treatments to lower the k value beyond 2.4 and to enhance mechanical strength of low-k dielectrics and novel integration schemes to preserve a low effective k value with an acceptable dielectric reliability are key challenges. New metallic barriers compatible with porous low-k films, thin seed layers, Cu filling, planarization and removal and impact on Cu microstructure, resistivity and electromigration will be investigated in sub-100nm pitch interconnect test structures. Research on Cu and low-k metrology will bring new insight in understanding the fundamental mechanisms that affect Cu/low-k interconnect properties during the integration process.

The interconnect program is part of a broader, strategic program on sub-45nm CMOS technology research, which is being executed with IMEC's core partners Infineon, Intel, Matsushita, Philips, Samsung, ST Microelectronics, and Texas Instruments, all world leading IDM companies.

"We are excited that we are now ready to move our materials-and-device research projects from the 200mm to the new 300mm fab and that we will be able to offer our partners also advanced interconnection technology processing by 2006 in our 300mm facility. The interconnect program enables our partners to cost effectively make an early assessment of the interconnect technology selection for the 32nm node," said Luc Van den

hove, Vice President Silicon Process and Device Technology at IMEC.

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