

# Development of durable MTJ under harsh environment for STT-MRAM at 1Xnm technology node

June 14 2019

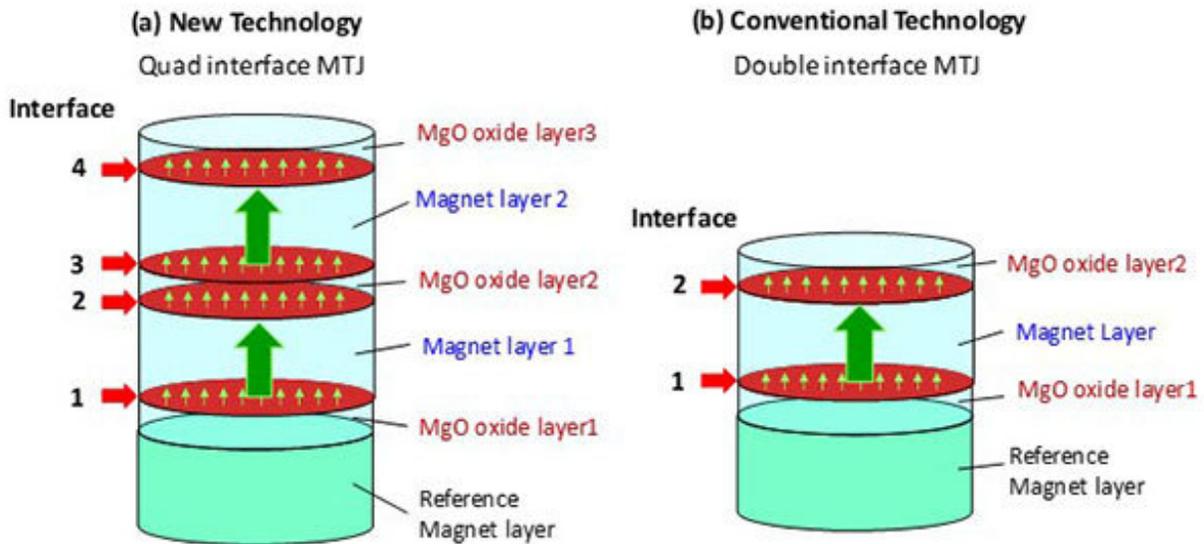


Figure 1: (a) The developed MTJ structure in this study compared with (b) the conventional MTJ structure. Credit: Tohoku University

Researchers at Tohoku University have announced the development of a

new magnetic tunnel junction, by which the team has demonstrated an extended retention time for digital information without an increase of the active power consumption.

Non-volatile memories are essential constituents in integrated circuits, because they can offer [low power consumption](#). Among proposed non-volatile memories, spin-transfer-torque magnetoresistive random access memory (STT-MRAM) has been intensively researched and developed, because of their high read/write speed, low voltage operation capability, and high endurance.

Currently, the application area of STT-MRAM is limited in consumer electronics. In order to use STT-MRAM in areas such as automotive and social infrastructure, it is vital to develop a magnetic tunnel junction (MTJ) with a high thermal stability factor that determines retention time for [digital information](#), while keeping the power consumption low.

The research team, led by Professor Tetsuo Endoh, has developed a new magnetic tunnel junction with a highly reliability for STT-MRAM at reduced dimensions of 1Xnm [technology](#) node. To increase the thermal stability factor, it is necessary to increase the interfacial magnetic anisotropy originating at the CoFeB/MgO interface.

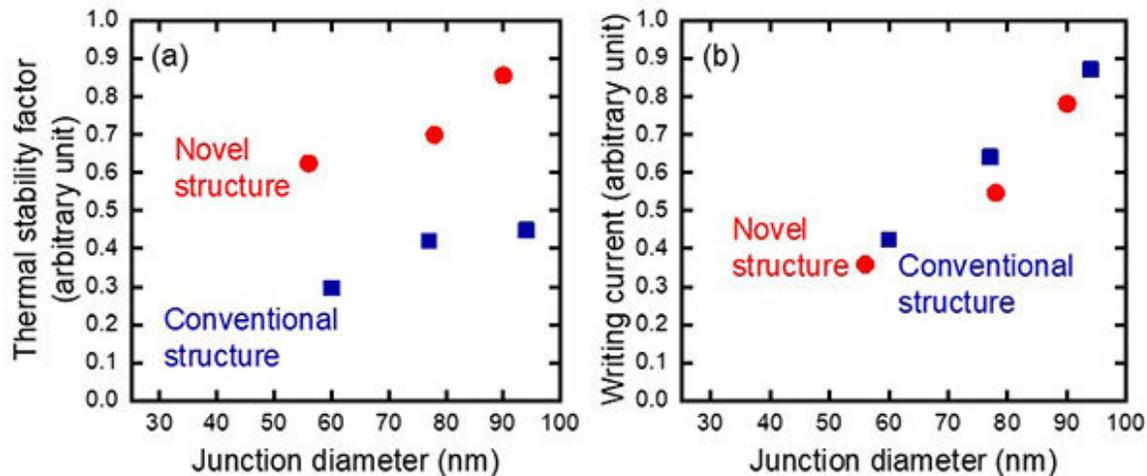


Figure 2: (a) Thermal stability factor of MTJs with the new structure compared with those with the conventional structure. (b) Writing current of MTJs with the new structure compared with those with the conventional structure. Credit: IEEE & Tohoku University

To increase the interfacial anisotropy, the research team has invented a structure with twice the number of CoFeB/MgO interfaces compared with a conventional one (Figs. 1a and 1b). Although the increase in the number of interfaces can enhance the thermal stability factor, it might also increase the writing current (the active power consumption) and degrade the tunnel magnetoresistance ratio of STT-MRAM cells, resulting in a lower reading operation frequency. The team has mitigated these effects by engineering the MTJ structure to keep the power consumption low and tunnel magnetoresistance ratio high.

The research team has demonstrated that the thermal stability factor can be increased by a factor of 1.5—2, without increasing the writing current and thus the active [power](#) consumption (Figs. 2a and 2b) or degrading

the [tunnel](#) magnetoresistance ratio.

Therefore, the research team is optimistic that this new MTJ technology can lead to a widening of application areas of STT-MRAM at 1Xnm technology node in harsh environments such as automotive and social infrastructure. The team has also adopted the same material set as those used in the STT-MRAM currently mass-produced, retaining compatibility with the existing process. The technology will simultaneously achieve high cost-effectiveness for mass-production.

This research is part of CIES's Industrial Affiliation on STT MRAM program and JST-OPERA program Grant Number JPMJOP1611, Japan. Results will be presented at this year's Symposia on VLSI Technology and Circuits which will be held in Kyoto, Japan from June 9 -14, 2019.

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**More information:** Title: Novel Quad interface MTJ technology and its first demonstration with high thermal stability and switching efficiency for STT-MRAM beyond 2Xnm

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