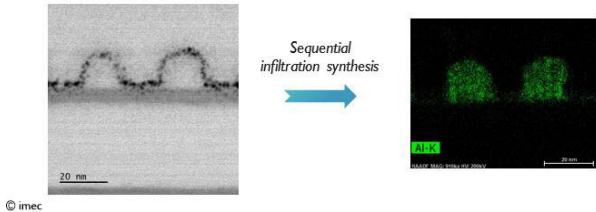


Sequential infiltration synthesis (SIS) significantly improves EUV patterning

25 February 2019, by Hanne Degans



TEM image of the photoresist pattern after lithography exposure (left) and TEM EDX signal from Aluminum for the photoresist pattern after the SIS step (right). Credit: IMEC

his week, at the SPIE Advanced Lithography conference 2019, imec, a world-leading research and innovation hub in nanoelectronics and digital technologies, demonstrates the positive impact of sequential infiltration synthesis (SIS) on the EUVL (extreme ultra-violet lithography) patterning process. This post-lithography technique is shown to significantly reduce stochastic nano-failures and line roughness, contributing to the introduction of EUVL patterning of future nodes". This work integrates recent advancements on metrology and etch, and on material developments, which will be presented in multiple papers at this week's 2019 SPIE Advanced Lithography Conference.

SIS is an existing technique, used in directed [self-assembly](#) (DSA) and now applied in EUV lithography, in which the photoresist is infiltrated with an inorganic element to make it harder and more robust, thereby enhancing the [patterning](#) performance on different parameters. Imec and partners show the first comparison between an EUVL-SIS and a standard EUVL patterning process demonstrating the benefits of SIS regarding roughness, nano-failure mitigation and local variability. When adding an SIS step during a full pattern transfer in a TiN layer, imec observed a improvement of 60 percent for intrafield local

critical dimension uniformity (LCDU) and 10 percent for line edge roughness compared to a reference process. These patterning enhancements are inherent properties of SIS. Also, the number of nanobreaks – a typical stochastic nano-failure – is reduced by at least one order of magnitude. Results were confirmed in an industrial relevant use case, showing reduced defectivity in a logic chip with a 20 percent smaller tip-to-tip critical dimension at a similar LCDU as a standard EUVL process.

The improvement SIS showcases on all parameters is indebted to imec's EUV lithography and metrology infrastructure and recent advancements in the field of process control, material and etch research. The current work brings these results and competences together in one paper, establishing SIS as a significant EUV patterning enhancement technique. The progress on each of the integrated aspects and SIS will be presented on the SPIE Advanced Lithography conference in multiple papers.

The work was performed in collaboration with ASM and ASML.

"The recent achievements with SIS for EUV [lithography](#) were enabled by the progress imec and its partners have made in various domains such as materials science, deposition, imaging, and metrology. This is a great example of how the integration of knowledge and combined efforts from multiple domains and ecosystem partners will enable a path to scale to N3 and beyond," said Greg McIntyre, director of advanced patterning at imec.

Provided by IMEC

APA citation: Sequential infiltration synthesis (SIS) significantly improves EUV patterning (2019, February 25) retrieved 21 April 2021 from <https://phys.org/news/2019-02-sequential-infiltration-synthesis-sis-significantly.html>

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