Sensing scheme improves accuracy when reading data from spin-based memory storage

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A voltage sensing scheme developed by researchers from Singapore could improve the accuracy of reading data from spin-based memory systems with only minimal modifications. The scheme responds dynamically to voltage changes in the system, so that it can better discern whether it is reading a binary on (1) or off (0) state.

The cutting-edge data storage technology, called spin-transfer torque magnetic random-access memory (STT-MRAM), encodes data using the intrinsic angular momentum of electrons—their spin, instead of their charge. Quang-Kien Trinh, Sergio Ruocco from the A*STAR Data Storage Institute and Massimo Alioto from the National University of Singapore are at the forefront of global efforts to prove that STT-MRAM can provide a fast, high-density, low-power alternative to existing charge-based memories.

"STT-MRAM is the leading candidate for future non-volatile, universal memory technology," says Trinh. "It could serve in consumer devices, corporate data centers, and even high-end critical applications such as unmanned vehicles, aircraft, and military."

In STT-MRAM systems, data bits are stored as either 1s or 0s by flipping the orientation of magnetized 'bitcells'. To read a bitcell, the system compares its own reference voltage to the 'bitline' voltage across the bitcell—the 1 or 0 state is then identified based on the difference between the two voltages, called the read margin.

However, "the memory read operation is recognized as one of the major roadblocks of this emerging technology," according to Trinh. The reference voltage frequently unintentionally flips the bitcell, or reads the wrong memory state if the read margin is small.

Trinh, Ruocco and Alioto realized that they could avoid read errors if they were to sense the bitline voltage and adjust the reference voltage in response, so that the read margin always remains high.

"Our new dynamic reference scheme generates two reference values, one for reading logic 0 and another for reading logic 1," explains Trinh. "In logic 0 state, a small readout signal is compared to a large reference value, while in logic 1 state, a large readout signal is compared to a small reference value."

The team's simulations suggest that their dynamic reference scheme could be incorporated into existing STT-MRAM systems with minimal modifications, and would reduce read errors by two orders of magnitude.

"We look forward to exploiting the synergy between our dynamic reference scheme and existing circuits," says Trinh. "We are also working on solutions to reduce the energy consumption and design complexity."

More information: Quang-Kien Trinh et al. Dynamic Reference Voltage Sensing Scheme for Read Margin Improvement in STT-MRAMs, *IEEE Transactions on Circuits and Systems I: Regular Papers* (2017). DOI: 10.1109/TCSI.2017.2749522

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