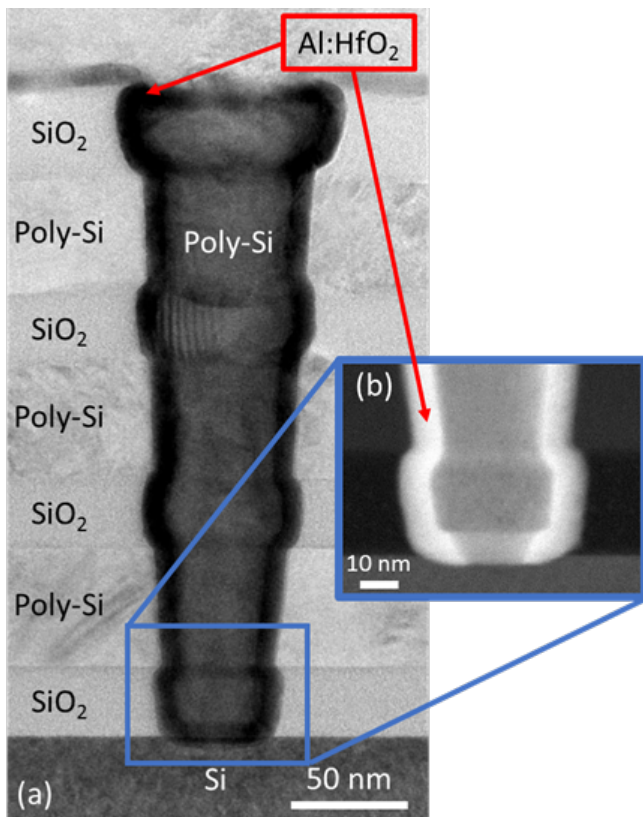


Breakthrough in CMOS-compatible ferroelectric memory

7 June 2017, by Hanne Degans



Credit: IMEC

Imec, the world-leading research and innovation hub in nanoelectronics and digital technology, announced today at the 2017 Symposia on VLSI Technology and Circuits the world's first demonstration of a vertically stacked ferroelectric Al doped HfO₂ device for NAND applications. Using a new material and a novel architecture, imec has created a non-volatile memory concept with attractive characteristics for power consumption, switching speed, scalability and retention. The achievement shows that ferroelectric memory is a highly promising technology at various points in the memory hierarchy, and as a new technology for storage class memory. Imec

will further develop the concept in collaboration with the world's leading producers of memory ICs.

Ferro-electric materials consist of crystals that exhibit spontaneous polarization; they can be in one of two states, which can be reversed with a suitable electric field. This non-volatile characteristic resembles ferromagnetism, after which they have been named. Discovered more than five decades ago, ferro-electric memory has always been considered ideal, due to its very low power needs, non-volatile character and high switching speed. However, issues with the complex [materials](#), the breakdown of the interfacial layer and bad retention characteristics have presented significant challenges. The recent discovery of a ferro-electric phase in HfO₂, a well-known and less complex material, has triggered a renewed interest in this memory concept.

"With HfO₂, there is now a material with which we can process ferro-electric memories that are fully CMOS compatible. This allows us to make a ferro-electric FET (FeFET) in both planar and vertical varieties," noted Jan Van Houdt, imec's chief scientist for memory technology. "We are working to overcome some of the remaining issues, such as retention, precise doping techniques and interface properties, in order to stabilize the ferro-electric phase. We are now confident that our FeFET concept has all the required characteristics. It is, in fact, suitable for both stand-alone and embedded memories at various points in the memory hierarchy, going all the way from non-volatile DRAM to Flash-like memories. It has particularly interesting characteristics for future storage-class memory, which will help overcome the current bottleneck caused by the differences in speed between fast processors and slower mass memory."

Imec recently presented the first, extremely positive results to its partners. The research center is now offering further development and industrialization of

the vertical FeFET as a program to all its memory partners, which include the world's major companies producing memory ICs.

"FeFETs can be used as a [technology](#) to build memory very similar to Flash-[memory](#), but with additional advantages for further scaling, simplified processing, and [power consumption](#)," added Van Houdt. "With our longstanding R&D and processing experience on advanced Flash, we are uniquely positioned to offer our partners a head start in this exciting opportunity. They can then decide how best to fit ferro-electric memories in their products and chips."

Provided by IMEC

APA citation: Breakthrough in CMOS-compatible ferroelectric memory (2017, June 7) retrieved 20 September 2021 from <https://phys.org/news/2017-06-breakthrough-cmos-compatible-ferroelectric-memory.html>

This document is subject to copyright. Apart from any fair dealing for the purpose of private study or research, no part may be reproduced without the written permission. The content is provided for information purposes only.