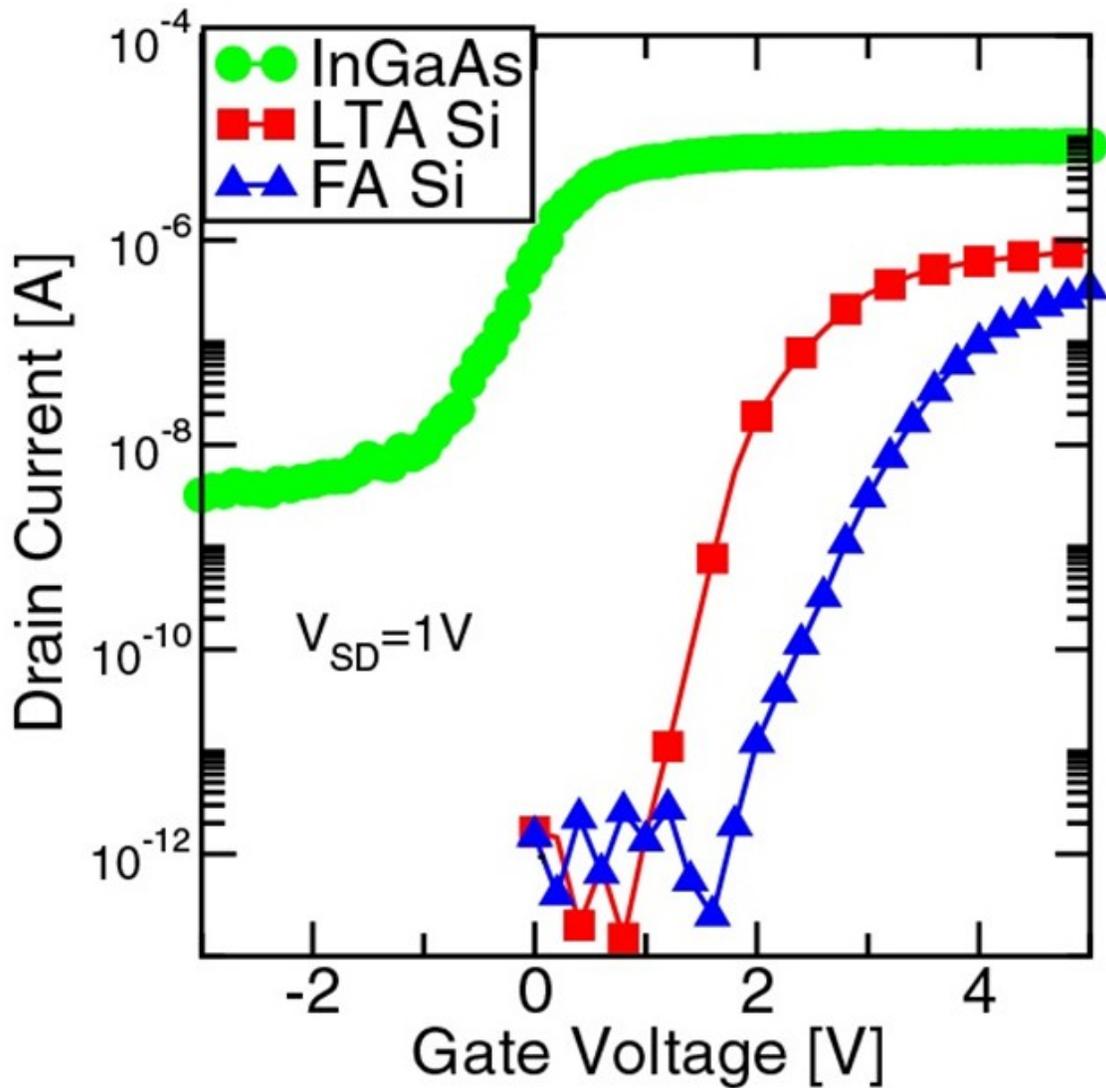


# Imec advances drive current in vertical 3D NAND memory devices

December 8 2015, by Hanne Degans



Typical ID-VG. In<sub>0.6</sub>Ga<sub>0.4</sub>As presents improved ID-VG characteristic. Ion/Ioff

ratio of 3 order of magnitude is sufficient for typical NAND operation.

At this week's IEEE IEDM conference, nano-electronics research center imec showed for the first time the integration of high mobility InGaAs as a channel material for 3D vertical NAND memory devices formed in the plug (holes) with the diameter down to 45nm. The new channel material improves transconductance (gm) and read current which is crucial to enable further VNAND cost reduction by adding additional layers in 3D vertical architecture.

Non-volatile 3D NAND flash [memory](#) technology is used to overcome the scaling issues in conventional planar NAND [flash memory technology](#), suffering from severe cell to cell interferences and read noise due to aggressively scaled dimensions. However, [current](#) 3D NAND devices, featuring a poly-Si channel, are characterized by drive current that will linearly decrease with the number of memory layers, which is not sustainable for long-term scaling. This is because the conduction in the poly-silicon channel material is ruled by grain size distribution and hampered by scattering at the grain boundaries and charged defects.

To boost the drive current in the channel, imec replaced the poly-Si channel material with InGaAs through a gate first-channel last approach. The channel was formed by metal organic vapor phase epitaxy (MOVPE) showing good III-V growth selectivity to silicon and holes filling properties down to 45nm. The resulting III-V devices proved to outperform the poly-Si devices in terms of on-state current (ION) and transconductance (gm), without degrading memory characteristics such as programming, erase and endurance.

"We are extremely pleased with these results, as they provide critical

knowledge of Flash memory operations with a III-V channel as well as of the III-V interface with the memory stack," stated An Steegen, Senior Vice president Process Technology at imec. "While these results are shown on full channels, they are an important stepping stone to develop industry-compatible macaroni-type III V channels."

Imec's research into advanced memory is performed in cooperation with imec's key partners in its core CMOS programs including Samsung, Micron-Intel, Toshiba-Sandisk, SK Hynix, TSMC, GlobalFoundries.

Provided by IMEC

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