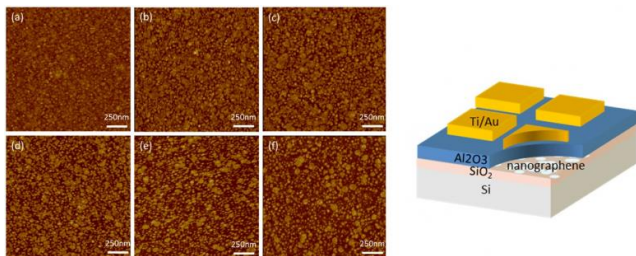


Nanographene charge trapping memory could further miniaturize flash

5 November 2015, by Lisa Zyga



(Left) Atomic force microscope image of the nanographene film with a high density of nanographene islands, which provide more charge-trapping sites to increase store capacity. (Right) Structure of the nanographene-based charge trapping memory. Credit: Meng, et al. ©2015 IOP Publishing

(Phys.org)—Flash memory—the data storage method often used in phones, computers, and other devices—is continually being miniaturized in order to improve device performance. In an attempt to reduce the short-circuiting that often occurs as memory cells become smaller and more closely packed, researchers have been investigating graphene-based charge trapping memory as an alternative to the traditional floating gate memory. Now in a new paper, researchers have developed a nanographene-based charge trapping memory that exhibits some of the best performance statistics for any such device reported to date.

The researchers, led by Dongxia Shi and Guangyu Zhang at the Chinese Academy of Sciences in Beijing (Zhang is also with the Collaborative Innovation Center of Quantum Matter in Beijing), have published a paper on the new memory device in a recent issue of *Nanotechnology*.

"As we all know, we are in an era of information explosion," Jianling Meng, from the Chinese Academy of Sciences and first author of the paper,

told *Phys.org*. "To improve data storage, it is necessary to decrease the footprint of a single node in order to achieve a high density of [data storage](#). Thus, it is a research hot point to keep shrinking flash memories. The biggest advantage for phones and computers having smaller flash memories is a larger storage capacity. Also, smaller [flash memories](#) can improve the program/erase speed of the data."

In general, shrinking the conventional floating gate memory cell is problematic because it causes short circuits. This happens because the floating gates where the electrons are stored are conductors, and so electrons can easily flow between them when the tiny cells are too close together. An advantage of charge trapping memory is that the charge trapping layer where the electrons are stored is an insulator, so shrinking these cells does not cause short circuits nearly to the extent that it does in [floating gate](#) memory cells.

In a charge trapping memory, electrons and other charge carriers are stored (or "trapped") in tiny defects in the graphene, which the researchers call "nanographene islands." The more nanographene islands, the more charge that can be stored, resulting in a higher memory capacity.

In the new study, the researchers developed a method for fabricating nanographene with a density estimated at more than a trillion (10^{12}) nanographene islands per square centimeter. Their strategy uses a technique called plasma etching to create large numbers of defects as well as extended defects along the edges of the main defects.

The large number of charge trapping sites provided by the defects enabled the researchers to fabricate a memory device with a very competitive memory performance. One measure of large capacitance is a large memory window, which indicates that a large number of [charge carriers](#) have been trapped.

Tests here revealed that the new memory has the largest ever memory window (9 volts) reported to date for a graphene-based charge trapping memory. In addition, this large memory window was maintained even after 1,000 program/erase cycles.

Overall, the researchers hope that this high-density memory will provide a path toward shrinking flash [memory](#) to even smaller scales.

"Our future research plan in this area is to realize a footprint as small as the tip of an atomic force microscope," Meng said.

More information: Jianling Meng, et al.

"Nanographene charge trapping memory with a large memory window." *Nanotechnology*. DOI: [10.1088/0957-4484/26/45/455704](https://doi.org/10.1088/0957-4484/26/45/455704)

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