Breakthrough Ultra-High-Speed Memory Technology That Solves Scaling Pace Limit in Embedded Memory Design

February 10 2005

NEC Electronics Corporation announced that they have succeeded in developing an ultra-high-speed memory technology that solves the design scaling limit caused by noise margin degradation in ultra-high speed embedded memory. Ultra-high-speed embedded memory devices are indispensable for next-generation, large-scale integrated (LSI) devices and high-speed computer systems. This new technology enables static random access memory (SRAM) to keep a scaling pace with complementary metal-oxide-semiconductor (CMOS) logic circuits.

This technology is mainly achieved using the following two techniques:

(1) To prevent data destruction caused by noise margin degradation, a data protection transistor is added to the conventional memory cell, which consists of six transistors.

(2) A layout design that combines a sensing circuit and a memory cell is developed to minimize the overhead area after the addition of the data protection transistor.

By applying the above two techniques to an SRAM device, its transistor threshold voltage can be lowered, resulting in an enhanced write cycle margin and acceleration of SRAM speed. This will enable SRAM devices to keep a scaling pace equivalent to that of CMOS logic circuits

in the 45-nanometer (nm) generation and beyond. In addition, as the newly developed SRAM shows the same delay-dependence on power supply as a CMOS logic circuit, it can be applied to dynamic-voltage scaling applications for power reduction.

Increases in device variation that accompany geometric scaling make LSI design difficult in the 45-nm generation and beyond. Within the composition elements of LSI design, SRAM is considered to be the most influenced by the increase in variation. Specifically, the noise margin in SRAM deteriorates. The noise margin is a parameter that guarantees stable data retention during read operations. In conventional SRAM design, the issue of noise margin is resolved by lowered power supply voltage and non-reduction of the threshold voltage. However, degradation in the write margin and operating speed will occur in the 45-nm generation and beyond when the ratio of the threshold voltage and power supply is increased.

"We are delighted that this breakthrough technology has finally solved the design scaling limit of ultra-high-speed embedded memory, which has been considered to hinder the 45-nm generation for many years. This technology places NEC one step ahead of the rest, and we will continue to aggressively develop this technology as a core technology for system-on-a-chip systems," said Dr. Masao Fukuma, vice president, R&D Unit, NEC Corporation.

As this technology achieves the high performance required of a system LSI chip, NEC and NEC Electronics will continue to strengthen their joint research and development in this area toward further enhancement of this key technology.