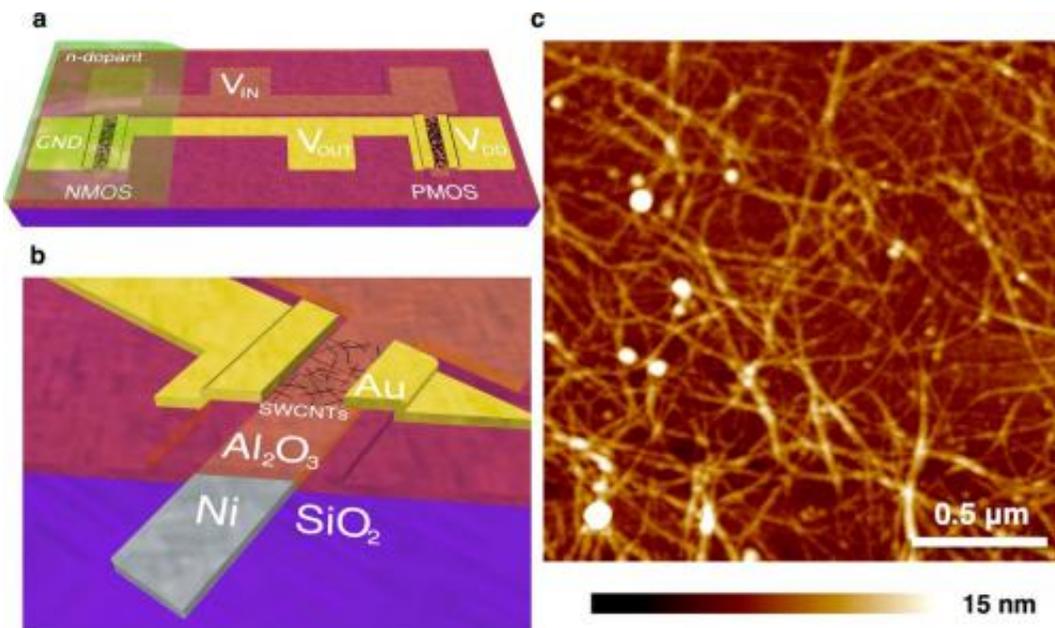


Carbon nanotube logic device operates on subnanowatt power

September 23 2013, by Lisa Zyga



Illustrations of (a) the CNT CMOS inverter and (b) a cross-section of an individual CNT transistor, including a 25-nm-thick Ni gate that enables ultralow power consumption. (c) Atomic force microscopy image of the CNT film morphology in the transistor channel region. Credit: Geier, et al. ©2013 American Chemical Society

(Phys.org) —Researchers have demonstrated a new carbon nanotube (CNT)-based logic device that consumes just 0.1 nanowatts (nW) in its static ON and OFF states, representing the lowest reported value by 3 orders of magnitude for CNT-based CMOS logic devices. The device

could serve as a building block for large-area, ultralow-power CNT logic circuits that can be used to realize a variety of nanoelectronics applications.

The researchers, Michael L. Geier, et al., at Northwestern University in Evanston, Illinois, and the University of Minnesota in Minneapolis, have published their paper on the subnanowatt CNT logic in a recent issue of *Nano Letters*.

"A modern-day integrated circuit has more than 1 billion transistors," coauthor Mark C. Hersam, Professor of Materials Science and Engineering, Chemistry, and Medicine at Northwestern University, told *Phys.org*. "Consequently, the [power dissipation](#) per transistor needs to be very low in order for the entire circuit to have a reasonable [power consumption](#). In fact, it is generally accepted that power consumption is the key limiting factor to achieving further increases in the complexity (i.e., number of transistors) in [integrated circuits](#)."

As the researchers explain, one of the biggest advantages of CMOS architecture is that it has intrinsically low power consumption. This benefit arises from the fact that, unlike other logic architectures, one of the two types of transistors (p-type or n-type) is turned off under steady state conditions in each logic gate in CMOS devices.

In order to fully take advantage of this potential for extremely low power consumption, the p-type and n-type transistors need to have precisely tuned and well-separated threshold voltages, which are the voltage levels that determine whether the device is ON or OFF. So far, this issue of the threshold voltages has not been addressed, and the researchers here identified it as the key challenge limiting the realization of highly integrated CNT-based CMOS electronics.

In their study, the researchers used a metal gate structure to achieve

symmetric and clearly separated threshold voltages for p-type and n-type CNT transistors, resulting in the ultralow power consumption. In the static states, in which the device is either ON or OFF, power consumption is less than 0.1 nW. At the midpoint of the transfer state, when both p-type and n-type transistors are simultaneously in the ON state, the voltage reaches its peak at 10 nW.

By connecting multiple CNT transistors in various configurations, the researchers demonstrated inverter, NAND and NOR logic gates. In the future, these gates can be integrated into complex circuits, where they can provide subnanowatt static power consumption along with the other advantages of CNTs, such as solution processability and flexibility.

"We are now working on making more complicated circuits, where we will have substantially more transistors and cascaded [logic gates](#)," Hersam said. "We also have an interest in combining carbon nanotubes with other emerging nanoelectronic materials in our lab (e.g., molybdenum disulfide [MoS₂])."

More information: Michael L. Geier, et al. "Subnanowatt Carbon Nanotube Complementary Logic Enabled by Threshold Voltage Control." *Nano Letters*. [DOI: 10.1021/nl402478p](https://doi.org/10.1021/nl402478p)

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