New design techniques enable extremely reliable medical devices

12 March 2012

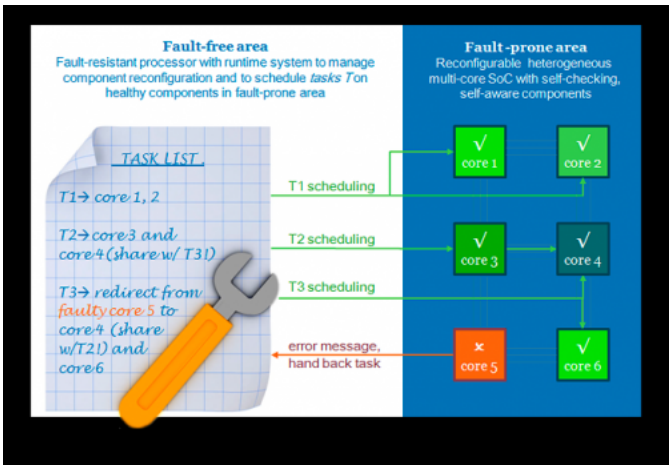
Implantable deep brain stimulators will benefit from the new Desyre approach for extremely reliable chips.

For pacemakers and other implantable medical devices there are three key factors: extreme reliability, small size, and long longevity. In the EU project Desyre, researchers tackle these issues with a new approach: building a reliable system on unreliable components.

To counter the increasing fault-rates expected in the next technology generations, Desyre develops new design techniques for future Systems-on-Chips to improve reliability while at the same time reducing power and performance overheads associated with fault-tolerance. Ioannis Sourdis, Assistant Professor in Computer Engineering at Chalmers, is the project leader of DeSyRe (on-Demand System Reliability).

“We focus on the design of future highly reliable Systems-on-Chips that consume far less power than other designs for high reliability systems,” he says. ”This approach allows by design devices that combine high reliability with small batteries and state-of-the-art longevity. It is perfect for safety-critical applications such as in implantable medical devices, for example pacemakers or deep brain stimulators that treat Parkinson’s disease”.

Research in reliable systems typically focuses on fail-safe mechanisms that use various redundancy schemes, in which sensitive subsystems are entirely doubled as a fail-safe. Checking for faults in the subsystem increases the energy consumption and decreases the performance of chips, as testing all subsystems cost time and energy.



The Desyre consortium takes a different approach, and separates the System-on-Chip (SoC) into two different areas: one which is extremely resistant to faults, and one area with fault-prone processing cores. The cores on the fault-prone area are interchangeable and the task of one core can easily be transferred to any of the other cores in case of a diagnosed malfunction. The fault-free part of the chip is responsible for monitoring the operation of the fault-prone part by performing sanity-checks of the processing cores, and for assuring that each core correctly handles an assigned sub-task.

“It sounds perhaps counterintuitive to design a highly reliable System-on-Chip on the basis of components that may fail, and yet this is exactly what we propose to do. Since our subsystems consist of small, interchangeable processing cores,

we can test and exclude individual cores while the function of the whole systems stays intact", says Gerard Rauwerda, CTO of Recore Systems, one of the industry partners of Desyre. "The beauty of the Desyre approach is that the system continues to do its job reliably, even if one or more cores fail, extending chip longevity."

The researchers expect this type of fault-tolerance to reduce energy consumption by at least ten to twenty percent compared to other redundancy schemes, while at the same time minimizing penalty on performance.

"People that need implantable medical devices will also benefit from this, as it pays off in a longer battery life and a postponed device replacement without any compromise to reliability," Ioannis Sourdis concludes.

Ioannis Sourdis explains the Desyre's approach on Monday March 12 in a tutorial on "Hardware and software design and verification for safety critical electronic systems" during the Date 2012 conference in Dresden, Germany.

Provided by Chalmer's University of Technology