Infineon Demonstrated New Tunneling FET Enabling Scalable Ultra-Low Voltage Processes in Standard Silicon Technology

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Infineon Demonstrated New Tunneling Field Effect Transistors Enabling Scalable Ultra-Low Voltage Processes in Standard Silicon Technology

At the 2004 IEEE International Electron Devices Meeting (IEDM) in San Francisco (December 13 – 15, 2004) scientists from Infineon Technologies AG introduced several papers representing outstanding achievements each. Together with the Technical University of Munich the company presented a new scalable transistor concept enabling low voltage digital and analog circuits. For the first time ever, complementary Tunneling Field Effect Transistors (TFETs) are fabricated in a standard silicon process with good performance for static and dynamic parameters.

“This is an important milestone on the way to transfer TFET research results into industrial applications,” states Doris Schmitt-Landsiedel, Professor at the Technical University of Munich. A low power logic family based on the new device was developed to exhibit the benefits with respect to extremely low power consumption and confirms the compatibility with the standard CMOS technology and circuit design. “Quantum mechanical tunneling, up to now regarded as a parasitic effect, is utilized for the operation of this device,” explains Thomas Nirschl, an Infineon engineer, who is presently on leave at the Technical University Munich as principal researcher in the TFET project.

For almost four decades, the progress of microelectronics, as defined by Moore's Law, has been based on the constant optimization of cost-efficient materials, processes and technologies. Leading semiconductor vendors like Infineon put strong efforts on further shrinking the process geometries. However, as indicated by the ITRS (International Technology Roadmap for Semiconductors), scaling of conventional bulk CMOS transistors becomes more and more difficult for the 45nm technology node (introduction planned in 2010) and beyond. Short channel effects are universal in standard MOSFETs and represent the gradual shorting together of the source and drain diffusions as the gate length reduces to small values near to the depletion layer widths of source and drain. This effect can be suppressed by high doping of the channel region, but at the expense of reduced electron mobility, lower speed and increased risk for avalanche breakdown. To maintain gate control of short MOSFET channels, the thickness of the gate dielectric must be scaled down, too. Due to the tunneling leakage through the conventional silicon dioxide new materials are needed. The integration of these high-k dielectrics is a severe challenge for CMOS process technology. In analog circuits, short channel effects affect the achievable amplification. Thus in the latest ITRS edition a section on analog applications is included, where the amplification factor gm/gDS is required to be larger than 100.

A potential solution for the described issues is the quantum-mechanical Tunneling Field Effect Transistor (TFET). Based on its different functional principle, the TFET offers a better potential to further scale the geometries and reduce the supply voltages compared to standard MOSFETs. The TFET structure as presented by Infineon and Technical University of Munich has a tunnel junction at the source side of the channel. In the non-conducting TFET a large pn-diode barrier exists between source and drain, which results in very low leakage currents. When a MOS channel is formed by forward biasing the gate, a Zener tunnel current evolves with a steep turn-on characteristic. The

researchers for the first time fabricated TFETs using a standard silicon process flow without any modification. Two different technology nodes (130nm and 90nm) are used to verify the scalability of the TFET working principle. A low-power TCMOS (TFET-CMOS) logic family developed at TU Munich can directly replace standard CMOS functions. Several demonstrator circuits were fabricated to verify on silicon the compatibility of the TFET and the standard MOSFET with respect to process flow and circuit functions. The TCMOS circuits reduce the static power consumption by up to a factor of 100 depending on the input vector.

With their exponential switching characteristic, TFETs are also ideal for integrated analog circuits. The reduction of short channel effects improves the analog properties of the device. Infineon measured an amplification factor of 110 for the TFET at an operation point of VDS = VGS = 0.6V. Hence the TFET enables ultra low voltage analog circuits.

The TFET working principle may also be applied to other MOS-gated devices. Due to its integrated substrate/well contact the TFET is perfectly suitable for partially depleted SOI (PDSOI) technologies. The floating body effect of standard PDSOI MOSFETs is eliminated. Process and device simulations have shown that the TFET is scalable down to 20nm without short channel effects. This allows using thicker gate oxide, and the necessity for high-k gate dielectrics is delayed.

Other papers by Infineon introduced at the IEDM meeting include:

-- Highly scalable sub 50nm vertical double gate DRAM cell
-- A highly manufacturable deep trench based DRAM cell layout
-- 3.3 ps SiGe bipolar technology
-- Low voltage flexible organic circuits with molecular gate dielectrics
-- Status and outlook of emerging non volatile memory technologies
-- Carbon Nanotubes for interconnect applications