Infineon Presents Cutting Edge Research Results in Non-Volatile Memory Technologies

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Munich, Germany – June 22, 2004 – Infineon Technologies is leading in the development of new non-volatile memory technologies. At the 2004 Symposia on VLSI Technologies and Circuits, June 15 - 19 in Honolulu, Hawaii, Infineon Technologies presented promising results on a broad range of non-volatile technologies for future memory products. Read about:

- 110nm NROM Technology for Code and Data Flash Products
- Infineon Explores FinFET Sub-40nm Oxide-Nitride-Oxide Transistors for High-Density Flash memory in the 16Gbit Range
- FeRAM - Small and Highly Scalable 3-Dimensional FeRAM Cell with Vertical Capacitor

110nm NROM Technology for Code and Data Flash Products

The increasing demand for portable consumer products like notebooks, digital still cameras, MP3 players and PDAs requires storing large amounts of data on removable memory, such as flash memory cards, CompactFlash Cards or USB devices. Non-volatile memories for such mass storage applications are cost driven, i.e. they require lowest cost/ bit solutions. By storing two separated bits in one cell the NROM technology, developed by Saifun, is highly attractive for cost competitive products. The recently introduced Twin-Flash products from Infineon Technologies Flash are built on

this 2-bit/cell architecture. The NROM cell is based on localized charge trapping in the nitride layer of an ONO (oxide nitride oxide) gate dielectric.

To maintain a small bit structure and low process complexity in the 110nm node, conceptual innovations need to be introduced. The new cell architecture presented by Infineon benefits from the advanced NMOS transistors' scaling concepts. Infineon presented a novel very competitive NROM generation with a bit size of only 0.043µm^2/bit at an 110nm design rule at VLSI Symposia. The concept features mainstream CMOS type cell devices in conjunction with a virtual ground array architecture. The new technology serves both advanced code flash and file storage memories of up to 2 Gbit/die.

Infineon Explores FinFET Sub-40nm Oxide-Nitride-Oxide Transistors for High-Density Flash memory in the 16Gbit Range

The scaling of floating gate flash memory transistors in the deep sub-100nm range faces serious challenges due to the thick tunnel oxides, which are required for reliable retention. Alternatively, charge trapping memory devices require inherently lower voltage and have good scaling properties.

At the VLSI Symposium, Infineon`s Corporate Research presented a novel FinFET (Fin Field Effect Transistor) based charge trapping memory technology suitable for very high integration densities for flash memory. These new memory transistors make use of three gates to improve the electrostatic channel control and thereby their scalability. The charge is stored in a nitride-trapping layer that is adjacent on the three sides of a fin. In contrast to traditional

floating gate cells, the tunnel oxide has excellent scaling properties since trapping layers are insensitive to single leakage paths. In this way, the Infineon researchers have achieved devices with very short gate length of 30nm - 40nm that would enable up to 16Gbit per die in a NAND-type array, which is about a factor of 10 above the currently available densities in single-level operation. Furthermore, this technology does not require any new materials and is therefore fully compatible with the well-established CMOS technology.

FeRAM - Small and Highly Scalable 3-Dimensional FeRAM Cell with Vertical Capacitor

In FeRAMs (Ferroelectric Random Access Memories) the remnant polarization of a ferroelectric thin film is used for information storage. Like MRAM, the FeRAM also represents a new paradigm in memory technologies. The advantages of FeRAM technology include SRAM-like fast read and write performance and low power consumption. This makes the technology well suited for applications in game consoles, cellular phones, mobile products and chip-cards.

Current FeRAMs still have a large cell size compared to DRAM or Flash, and development of a small and competitive FeRAM cell is therefore the key challenge. With the most widely pursued planar FeRAM cell concepts, only structural cell sizes down to ~10F2 are achievable, with F being the minimum feature size of the process. In addition, planar FeRAM cells have a limited shrinkability. In order to address these deficiencies, Infineon and Toshiba presented at the VLSI Symposium a novel chain FeRAM cell concept using a new 3-dimensional vertical capacitor. This novel cell concept is highly scalable and enables structural cell sizes down to 4F2.

In the vertical capacitor FeRAM cell presented by the researchers, the unit cell contains one transistor and one ferroelectric capacitor, which are connected in parallel. The contacts to the transistor and the vertical electrodes of the capacitor are shared among neighboring cells resulting in the compact cell structure. First promising results for this innovative cell concept were presented at the Symposium.

The original press release can be found here.