

New hardware boosts communication speed on multi-core chips

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Computer engineers at North Carolina State University have developed hardware that allows programs to operate more efficiently by significantly boosting the speed at which the "cores" on a computer chip communicate with each other.

The core, or [central processing unit](#), is the brain of a computer chip; most chips currently contain between four and eight cores. In order to perform a task more quickly using multiple cores on a single chip, those cores need to communicate with each other. But there are no direct ways for cores to communicate. Instead, one core sends data to memory and another core retrieves it using [software](#) algorithms.

"Our technology is more efficient because it provides a single instruction to send data to another core, which is six times faster than the best state-of-the-art software we could find," says Dr. James Tuck, an assistant professor of electrical and [computer engineering](#) at NC State and co-author of a paper describing the research. Tuck explains that the technology, called HAQu, is "not [hardware](#) designed to communicate data on its own, but is hardware that expedites data-sharing using existing data paths on a computer chip." Because HAQu uses these existing data paths, the research team compared it to software communication tools - even though it is a piece of hardware.

HAQu is also more energy efficient. "It actually consumes more power when operating but, because it runs so much more quickly, the overall energy consumption of the chip actually decreases," Tuck says.

The next step for the research team is to incorporate the hardware into a prototype system to demonstrate its utility in a complex software environment.

More information: The paper, "HAQu: Hardware-Accelerated Queueing for Fine-Grained Threading on a Chip Multiprocessor," is co-authored by Tuck, NC State Ph.D. students Sanghoon Lee and Devesh Tiwari, and Dr. Yan Solihin, an associate professor of electrical and computer engineering at NC State. The paper will be presented Feb. 14 at the International Symposium on High-Performance Computer Architecture in San Antonio, Texas. The research was funded, in part, by the National Science Foundation.

Provided by North Carolina State University

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