World´s Fastest 6bit Flash Analog-to-Digital Converter in 0.13µm Standard CMOS Technology

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Munich/Germany and Honolulu/Hawaii – June 21, 2004 – At the 2004 Symposia on VLSI Technologies and Circuits, June 15 - 19 in Honolulu, Hawaii, USA, Infineon Technologies demonstrated several milestones for leading edge semiconductor technology. Amongst them is a 4GS/s 6bit Flash analog-to-digital converter (ADC) in standard CMOS technology. This innovative chip design represents the fastest 6bit Analog-to-Digital converter manufactured in a standard CMOS process with the related benefits on easy and cost effective integration.

Today's high data transfer rates in various serial communication applications such as the read channels of hard disks rely on digital signal processing circuitry. These circuits require high speed ADCs to provide the interface between the analog and digital parts of the system. It is desirable to realize these integrated circuits in standard CMOS technologies to allow low cost production and monolithically integration of ADC and digital signal processor (DSP).

At VLSI 2004 Infineon presented a high-performance 4GS/s 6bit flash ADC with 8bit output realized in a 0.13µm standard CMOS technology. The outputs of the 255 small-area comparators with comparatively large input offsets are averaged by a fault tolerant thermometer-to-binary converter. The ADC also uses an on-chip low jitter VCO (voltage controlled oscillator) for clock provision and consumes 990mW at a single supply voltage of 1.5V.

In a classical n-bit flash ADC only 2n-1 comparators with low input offset voltages are used to generate a perfect bubble-free thermometer code at the output of the comparator bench. To guarantee the demanded low input offset voltage, large active device areas must be used to reduce the effect of device mismatch within the comparators.
In contrast to this traditional approach, the new Infineon ADC with 6bit linearity uses 255 comparators with small active area. As a consequence, the input offset voltages are in fact higher, and a bubble-free thermometer code at the output of the comparator bench is not obtained, but the small sized comparators can be optimised for maximum operation speed. Device mismatch related errors in the code at the output of the comparator bench are compensated by averaging in the digital domain, which can be accomplished at highest speeds. The comparator outputs are connected to a fault-tolerant thermometer-to-binary converter with an 8bit resolution output.

In high-speed ADCs (>1GS/s), clock generation and distribution is a crucial point to meet the desired resolution. Since an uncertainty of the clock signal (jitter) directly translates into a reduction of the resolution of the system, the jitter has to be kept as small as possible. At an input frequency of 1GHz, a 6bit ADC needs to be clocked with a jitter of less than 1ps. Therefore, the new ADC comprises an on-chip LC oscillator with low jitter, which provides a complementary sinusoidal signal at a frequency of 4 GHz.

The measurement results of the new flash ADC clearly demonstrate its full functionality. Since only standard digital transistors are used, the ADC can easily be monolithically integrated in a signal processor without the need for analog process options. Furthermore, the RF clock signal is generated on-chip and only a single supply voltage of 1.5V is used. In addition, the combination of the ADC with a digital signal processor offers the advantage of an increased resolution of the system, since a digital calibration can be implemented easily. The presented

ADC circuit is an important milestone on the way to powerful mixed signal devices to meet the requirements of next generation communication products.

The original press release can be found here.

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