Intel, Micron Achieve Industry's Most Efficient NAND Product Using 3-Bit-Per-Cell Technology

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Intel Corporation and Micron Technology today announced the development of a new 3-bit-per-cell (3bpc) multi-level cell (MLC) NAND technology, leveraging their award-winning 34-nanometer NAND process. The chips are typically used in consumer storage devices such as flash cards and USB drives, where high density and cost-efficiency are paramount.

Designed and manufactured by IM Flash Technologies (IMFT), their NAND flash joint venture, the new 3bpc NAND technology produces the industry's smallest and most cost-effective 32-gigabit (Gb) chip that is currently available on the market. The 32Gb 3bpc NAND chip is 126mm².

Micron is currently sampling and will be in mass production in the fourth quarter 2009. With the companies' continuing to focus on the next process shrink, 3bpc NAND technology is an important piece of their product strategy and is an effective approach in serving key market segments.

"We see 3bpc NAND technology as an important piece of our roadmap," said Brian Shirley, vice president of Micron's memory group. "We also continue to move forward on further shrinks in NAND that will provide our customers with a world-leading portfolio of products for many years to come. Today's announcement further highlights that Micron and Intel have made great strides in 34-nanometer NAND, and we look forward to introducing our 2xnm technology later this year."

Source: Intel (news : web)

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