

# New 167-processor chip is super-fast, ultra energy-efficient

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A new, extremely energy-efficient processor chip that provides breakthrough speeds for a variety of computing tasks has been designed by a group at the University of California, Davis. The chip, dubbed ASAP, is ultra-small, fully reprogrammable and highly configurable, so it can be widely adapted to a number of applications.

The [chip](#) is designed for digital signal processing. While not the principal kind of processor chip used in desktop computers, digital signal processing chips are found in a myriad of everyday and specialized devices such as cell phones, MP3 music players, video equipment, anti-lock brakes and ultrasound and MRI medical imaging machines.

Maximum clock speed for the 167-processor ASAP is 1.2 gigahertz (GHz), but at slower speeds its energy efficiency soars. Twelve chips working together could perform more than half-a-trillion operations per second (.52 Tera-ops/sec) while using less power than a 7-watt light bulb.

"A battery powering this chip will typically last from several times to 75 times longer than it would under the same workload when powering some of the common commercially available digital [signal processing](#) chips," said Bevan Baas, associate professor of electrical and [computer engineering](#) and leader of the design team. "At the same time, with our targeted applications, we're getting several times to 10 times better speed than what is currently available — all with a much smaller chip. To the best of our knowledge, this is the highest clock-rate processor chip designed at any university."

Built with what's known as 65 nanometer CMOS technology, the ASAP measures only about one-fifth of an inch (less than 6 mm) on a side. It could be made even smaller if the number of processors were reduced, which could make it suitable for applications like retinal implants and hearing aids

that require extreme miniaturization, Baas said.

Also, the small size keeps production costs low: a rule of thumb in the industry is that for every doubling of size, manufacturing costs per chip will be much more than twice as high.

Although the chip is built with industry-standard fabrication technology and design tools, it embodies a number of novel architectural and circuit features, Baas explained. Throughout the design process, his group took energy efficiency and high speed into consideration. "These were two of our main objectives, which we never gave up on during the planning stages. And all those choices added up," he said.

Multi-processor chips like the ASAP are part of a growing trend in chip design. With the need for increasing speed driving the industry, designing high-speed processor chips has become a daunting task due to several factors, including complexity of design, but also because the faster a processor works, the more it heats up. In a multi-processor chip, the work load is spread over many processors working in parallel, so heating and energy consumption can be kept in check.

Baas' group has written a number of software applications for the chip, which has been fabricated by the international electronics company STMicrotronics. It took one student just three months to write "a fully compliant Wi-Fi transmitter," Baas said. They have also written a Wi-Fi receiver and several complex components of an H.264 video encoder. After testing the chip extensively, it has worked without a glitch, Baas added.

The group made a brief announcement about the chip in June 2008 at the Symposium on VLSI Circuits in Honolulu, and details of its design have just been published in the April issue of *IEEE Journal of Solid-State Circuits*.

"The paper makes key ideas behind the design

available to industry and university researchers," Baas said. "Now our group plans to continue developing software and programming tools for the chip while exploring ideas for the next generation."

Source: University of California - Davis

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