UCLA scientists working to create smaller, faster integrated circuits

19 December 2007

Integrated circuits are the "brain" in computers, cell phones, DVD players, iPhones, personal digital assistants, automobiles' navigation systems and anti-lock brakes, and many other electronic devices.

A team of UCLA scientists has now demonstrated substantial improvements in integrated circuits, achieved not by costly improvements in manufacturing but by improved computer-aided design software based on better mathematical algorithms.

"We can get circuits designed with 30 percent less wire length using improved optimization than what we had demonstrated three years ago, based on circuits that were samples from industry," said Jason Cong, UCLA professor and chair of computer science. "We believe that when you apply these methods to current industry circuits, you will see similar gains. Industry says even 5 percent is very significant.

"We are showing there is another way to make major improvements, with better design and better architecture," added Cong, who has collaborated for nearly a decade with Tony Chan, UCLA professor of mathematics and the National Science Foundation's assistant director for mathematics and physical sciences.

The traditional way to achieve smaller, faster integrated circuits — also known as silicon chips — is by building smaller and smaller transistors and thinner wires. While the computer industry has made smaller, improved devices, Cong, Chan and their colleagues are improving the design of the chip itself.

A goal of the collaboration is the development of silicon chips that are faster and cheaper and consume less power than the current generation of chips, said Cong, who is also a member of the California NanoSystems Institute at UCLA.

"We think optimizing chip design is an exciting direction," he said.

Integrated circuits have a series of interconnected, nanosize nodes; the locations of the nodes on the chip's surface are very important because they can minimize the wire length on which the signal travels.

Nodes include tiny "logic gates," as well as much larger memory blocks and other functional blocks. There are tens of millions of nodes on a chip.

"We have found there is a huge amount of room for improvement in the physical design of the chip itself, including where nodes are placed," said UCLA mathematics graduate student Eric Radke, who works with Chan and Cong. "We want to minimize the wire length in each node."

A challenge, Cong said, is "how do you place the nodes on a two-dimensional surface with big pieces and small pieces that are all connected to one another" It's like a jigsaw puzzle with millions of pieces. How do you place them to minimize the total interconnections (wires) among them""

"It's fairly easy to model this problem mathematically," Radke said. "You can think of the nodes as points on a giant graph, and you can think of the interconnects as hyper-edges that connect more than two nodes. We can use mathematics to determine how the placement problem should be solved. We use a mathematical technique called multiscale methods, in which we group nodes together until we get a mathematical problem that is small enough to solve."

Chan and Radke design algorithms for computer software to improve the placement of the nodes and are using differential equations that they build into the algorithms. The scientists expect that the research will lead to improved software for enhanced chip design. Cong's laboratory has found

strong evidence that existing computer-aided programs for integrated circuit design are far from optimal.

Chan and Radke are now working to minimize the amount of time it takes a signal to get through a processor.

Research by Chan, Cong and their graduate students won the 2005 award for best paper at the International Symposium of Physical Design (ISPD). Their placement software, developed together with their former students Kenton Sze and Min Xie, also produced the best wire-length results in the 2006 Circuit Placement Contest organized by ISPD.

Chan and Cong are also working with Lieven Vandenberghe, UCLA professor and vice chair of electrical engineering, as well as computer science graduate student Guojie Luo and electrical engineering graduate student John Lee.

"It's great to come to the meetings and hear everybody's ideas because everybody comes from a different background," Radke said.

Source: University of California - Los Angeles