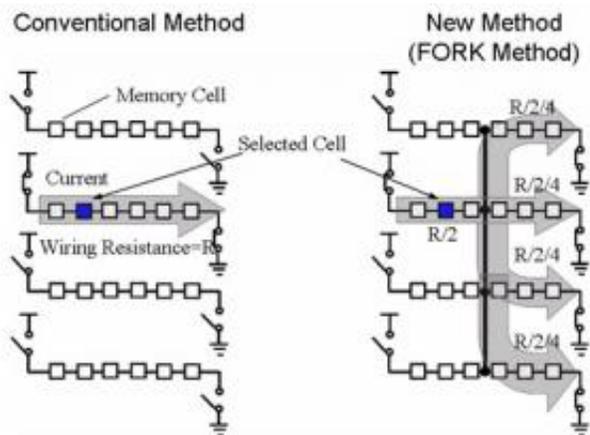


Toshiba and NEC Develop World's Fastest, Highest Density MRAM

February 7 2006



Mechanism of reduced electrical resistance in wiring for writing: The resistance per wiring was reduced by 38% by adopting new wiring method which forks writing current.

Toshiba Corporation and NEC Corporation today announced that they have developed a magnetoresistive random access memory (MRAM) that combines the highest density with the fastest read and write speed yet achieved. The new MRAM achieves a 16-megabit density and a read and write speed of 200-megabytes a second, and also secures low voltage operation of 1.8V.

A major challenge of MRAM development to date has been the acceleration of read speeds: the current drive circuit used to generate the magnetic field for writing degrades read operation from memory cells.

The new MRAM has an improved circuit design that divides the current paths for reading and writing, realizing a faster read speed. It also reduces equivalent resistance in wiring by approximately 38% by forking the write current. These innovations together achieve a read and write speed of 200-megabytes a second and a cycle time of 34 nanoseconds — both the world's best performance for MRAM. This performance is underlined by a low operating voltage of only 1.8V, the ideal voltage for mobile digital products.

Alongside advances in performance, the new MRAM achieves advances in chip size. Toshiba and NEC have introduced the above mentioned technologies and optimized overall circuit design, achieving a chip that, at 78.7mm², is approximately 30% smaller than its equivalent without the new circuit design. The new MRAM is the world's smallest in the 16-megabit era.

MRAM is expected to be a next-generation non-volatile memory that retains data when powered off and that achieves fast random access speeds and unlimited endurance in operation.

Development of these new MRAM technologies was supported by grants from Japan's New Energy and Industrial Technology Development Organization (NEDO).

Full details of the new technology were presented on February 6 at ISSCC (International Solid-State Circuits Conference) 2006 in San Francisco, USA.

Source: NEC

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