

Shanghai Research Center for Integrated Circuit Design and Cadence Introduce New CPU/DSP Core-Based Methodology for SOC

31 August 2004

[Cadence Research](#) Design Systems, Inc. and the Shanghai Center For Integrated Circuit Design (ICC), China's first national integrated circuit (IC) design industrialization base founded by China's Ministry of Science and Technology, today announced the availability of the ICC-Cadence CPU/digital signal processing (DSP) system-on-chip (SoC) reference methodology. The reference methodology, which includes the Cadence® Encounter digital implementation platform, Incisive™ functional verification platform and CoWare software tools for electronic system-level design and verification, is the first to offer rapid and predictable implementation of SoC chip designs for the expanding IC industry in China.

"We are pleased to cooperate with Cadence to cultivate the mainstream design industry in China through this SoC reference methodology project," said Ye Wang, vice director of ICC. "This methodology enables a proven design flow for our mutual customers to quickstart, follow-through and complete their SoC chip designs effectively. This methodology reduces the risk of design failures, ensuring predictable performance and reducing the overall development time to silicon. These elements are particularly important for China's local enterprises to grow their SoC chip business when they are young."

Based on the Cadence Encounter™ digital IC design and Incisive functional verification platforms, the reference methodology was built upon CPU and DSP cores from leading processor IP providers. The implementation flow was validated with several leading foundries on their 0.18-micron processes. The tools supported in the reference methodology include NC-Sim, Conformal®-ASIC, Nano Encounter™, CeltIC™, Fire & Ice® QXC, VoltageStorm®, SignalStorm® and CoWare ConvergenSC Advanced System

Designer through a Cadence and CoWare strategic partnership.

"The ability to implement SoC design quickly and meet the market timeframe is critical for success in today's China IC markets," said Wayne Tang, president of Cadence China operations. "This reference methodology provides the right mix of technologies to address the needs of China's IC design engineers. The result of our successful collaboration with ICC is to provide a complete, one-stop CPU-based SoC solution. It also symbolizes the Cadence commitment to the China IC industry."

APA citation: Shanghai Research Center for Integrated Circuit Design and Cadence Introduce New CPU/DSP Core-Based Methodology for SOC (2004, August 31) retrieved 27 October 2020 from <https://phys.org/news/2004-08-shanghai-center-circuit-cadence-cpudsp.html>

This document is subject to copyright. Apart from any fair dealing for the purpose of private study or research, no part may be reproduced without the written permission. The content is provided for information purposes only.