Scientists discover way to 'grow' sub-nanometer sized transistors

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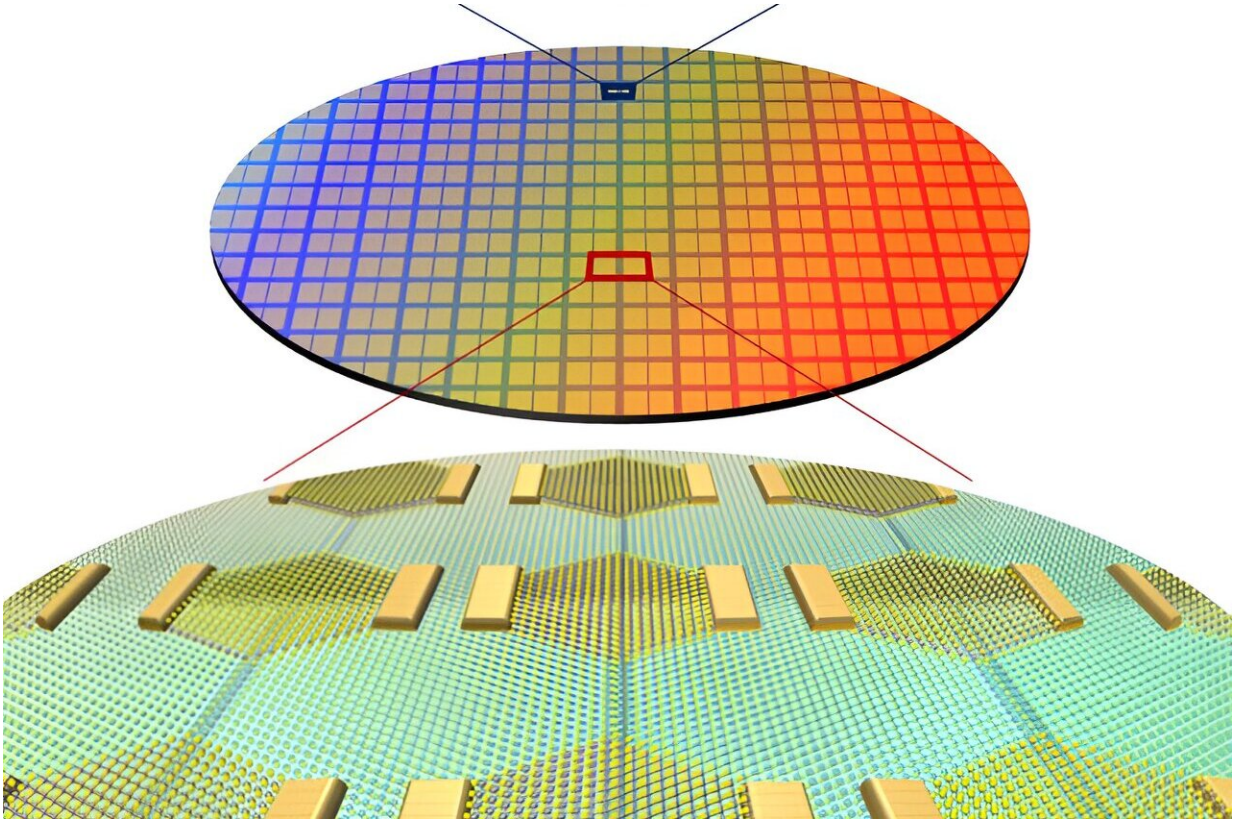


This figure depicts the synthesis of metallic 1D mirror twin boundaries through Van der Waals epitaxial growth (top) and the large-area 2D semiconductor integrated circuit constructed based on these boundaries (bottom). By controlling the crystal structure of molybdenum disulfide at the atomic level using Van der Waals epitaxial growth, metallic 1D mirror twin boundaries were freely synthesized in desired locations on a large scale. These boundaries were applied as gate electrodes to implement ultra-miniaturized 2D semiconductor transistors with channel lengths at the atomic scale. Credit: Institute for Basic Science

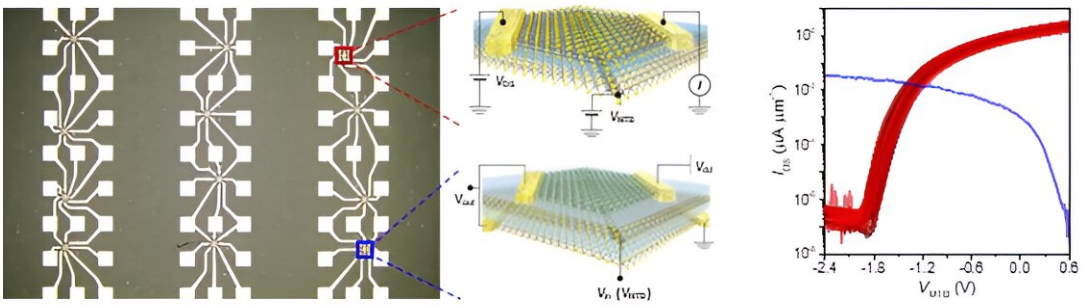
A research team led by Director Jo Moon-Ho of the Center for Van der Waals Quantum Solids within the Institute for Basic Science (IBS) has implemented a novel method to achieve epitaxial growth of 1D metallic materials with a width of less than 1 nm. The group applied this process to develop a new structure for 2D semiconductor logic circuits. Notably, they used the 1D metals as a gate electrode of the ultra-miniaturized transistor.

This research appears in *Nature Nanotechnology*.

Integrated devices based on two-dimensional (2D) semiconductors, which exhibit excellent properties even at the ultimate limit of material thickness down to the atomic scale, are a major focus of basic and applied research worldwide. However, realizing such ultra-miniaturized transistor devices that can control the electron movement within a few nanometers, let alone developing the manufacturing process for these integrated circuits, has been met with significant technical challenges.

The degree of integration in semiconductor devices is determined by the width and control efficiency of the gate electrode, which controls the flow of electrons in the transistor. In conventional semiconductor fabrication processes, reducing the gate length below a few nanometers is impossible due to the limitations of lithography resolution.

To solve this technical problem, the research team leveraged the fact that the mirror twin boundary (MTB) of molybdenum disulfide (MoS_2), a 2D semiconductor, is a 1D metal with a width of only 0.4 nm. They used this as a gate electrode to overcome the limitations of the lithography process.



This figure shows an optical microscope image of the integrated circuit based on 1D mirror twin boundary gates (left), a schematic of the ultra-miniaturized transistor and inverter devices that constitute the circuit (center), and the performance evaluation of these devices (right). The 1D mirror twin boundary process developed by the research team was not limited to the miniaturization of individual devices but was successfully used to construct large-area, highly integrated electronic circuits. Credit: Institute for Basic Science

In this study, the 1D MTB metallic phase was achieved by controlling the crystal structure of the existing 2D semiconductor at the atomic level, transforming it into a 1D MTB. This represents a significant breakthrough not only for next-generation semiconductor technology but also for basic materials science, as it demonstrates the large-area synthesis of new material phases through artificial control of crystal structures.

The International Roadmap for Devices and Systems (IRDS) by the IEEE predicts semiconductor node technology to reach around 0.5 nm by 2037, with transistor gate lengths of 12 nm. The research team demonstrated that the channel width modulated by the electric field applied from the 1D MTB gate can be as small as 3.9 nm, significantly exceeding the futuristic prediction.

The 1D MTB-based transistor developed by the research team also offers advantages in circuit performance. Technologies like FinFET or Gate-All-Around, adopted for the miniaturization of silicon semiconductor devices, suffer from parasitic capacitance due to their complex device structures, leading to instability in highly integrated circuits. In contrast, the 1D MTB-based transistor can minimize parasitic capacitance due to its simple structure and extremely narrow gate width.

Director Jo Moon-Ho commented, "The 1D metallic phase achieved through epitaxial growth is a new material process that can be applied to ultra-miniaturized semiconductor processes. It is expected to become a key technology for developing various low-power, high-performance electronic devices in the future."

More information: Integrated 1D epitaxial mirror twin boundaries for ultra-scaled 2D MoS2 field-effect transistors, *Nature Nanotechnology* (2024). DOI: 10.1038/s41565-024-01706-1

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