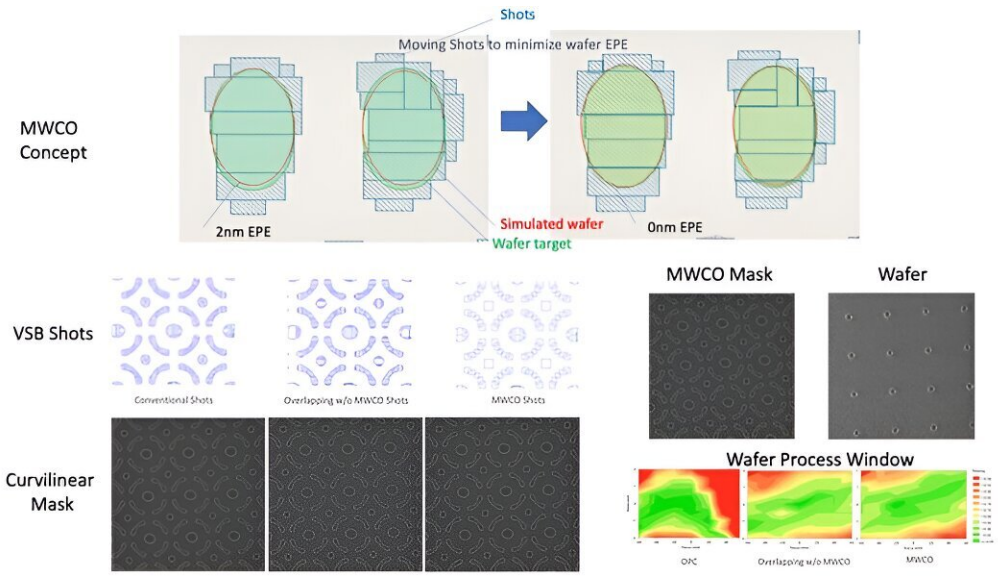
Throwing lithography a curve: Research introduces mask wafer co-optimization method

February 20 2024



Concept of mask/wafer co-optimization by moving the shot with mask and wafer double simulation to minimize wafer error. VSB shot configurations and its corresponding pattens on mask. MWCO mask and its wafer print. Wafer Process Windows shows MWCO improved process window by 2x. Process window is a key measurement of wafer print quality. Credit: *Journal of Micro/Nanopatterning, Materials, and Metrology* (2024). DOI: 10.1117/1.JMM.23.1.011207

At the heart of advancing semiconductor chip technology lies a critical

challenge: creating smaller, more efficient electronic components. This challenge is particularly evident in the field of lithography, the process used to create intricate patterns on semiconductor materials (called wafers) for the production of chips.

Lithography uses a kind of template, called a photomask—or just mask—for creating patterns on semiconductor wafers. The industry is always looking for methods that improve resolution and manufacturability for both masks and wafers, which will produce faster chips with higher yield of properly functioning chips.

Computational lithography techniques that improve resolution and pattern fidelity, such as optical proximity correction (OPC), have made significant strides in addressing these challenges by modifying the individual mask patterns to improve both mask and wafer printing.

Inverse lithography technology (ILT)—a mathematically rigorous inverse approach that determines the mask shapes that will produce the desired on-wafer results—has been seen as a promising solution to many of the challenges of lithography for advanced chips. Since its introduction more than a decade ago, there have been numerous studies that demonstrate that curvilinear ILT mask shapes, in particular, produce the best wafer results.

However, until recently, the runtimes associated with this computational technique have limited its practical application to critical "hotspots" on chips. In 2019, an entirely new, purpose-built system was proposed, including a unique GPU-accelerated approach that emulates a single, giant GPU/CPU pair that can compute an entire full-chip ILT solution at once. This novel approach, systematically designed for ILT and GPU acceleration, made full-chip ILT a practical reality in production.

However, this approach relied on multi-beam mask writing, an important

new development in mask writing that is pixel-based and so is shape-agnostic in terms of write-time. The question that remained was if the benefits of full-chip, curvilinear ILT could be extended to the variable shaped beam (VSB) mask writers that write rectilinear (and sometimes triangle) shapes rather than pixels, and that make up the majority of mask writers around the world today.

While VSB writers create larger rectangular shapes quickly by writing one rectangular shot at a time, complex mask patterns can be an issue because the high number of small rectangles needed to create them would take too long to write.

Reporting their work in the *Journal of Micro/Nanopatterning, Materials, and Metrology*, the team at D2S, Inc. invented a method called mask wafer co-optimization (MWCO) with three insights: the mask writer and the wafer scanner are both low-pass filters; overlapping shots guided by mask/wafer simulation can create curvilinear shapes with fewer shots; by targeting the wafer pattern, instead of the mask pattern, one can create much simpler shots to print the correct wafer pattern. By using this double simulation, wafer print quality is iteratively optimized while manipulating VSB shot edges to produce rectilinear target mask shapes that are known to be writable on a VSB writer, with a known and acceptable shot count.

D2S and Micron Technology have demonstrated MWCO can reduce the wafer variation by 3x, and can improve the wafer process window by 2x compared to Micron OPC, indicating a substantial improvement in the precision and reliability of the lithography process. The write time for a full curvilinear ILT mask would be less than 12 hours, satisfying high-volume production requirements.

This means that all semiconductor manufacturers now can produce chips that are not only smaller but also have higher performance and lower

power consumption, even if they do not have access to a multi-beam mask writer.

More information: Linyong (Leo) Pang et al, Make the impossible possible: use variable-shaped beam mask writers and curvilinear full-chip inverse lithography technology for 193i contacts/vias with mask-wafer co-optimization, *Journal of Micro/Nanopatterning, Materials, and Metrology* (2024). DOI: 10.1117/1.JMM.23.1.011207

Provided by SPIE