Researchers look at thermal stabilization in photonic packages
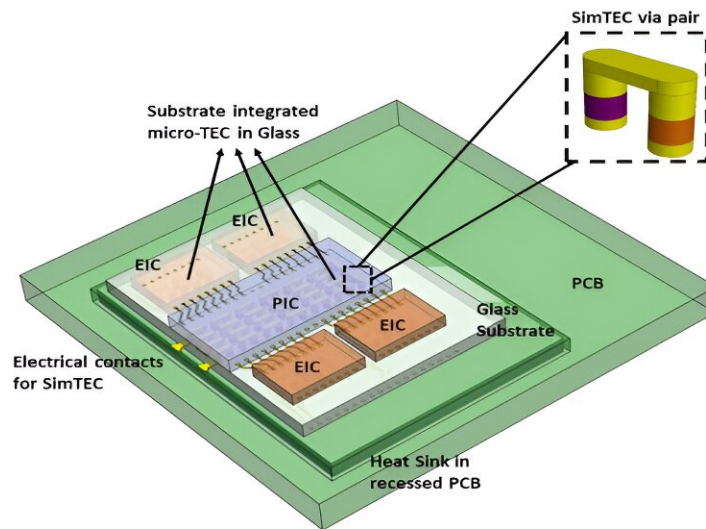
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Diagram showing the SimTEC architecture in glass substrate with SimTEC vias operating in the central region of the electronic chips (EIC) and photonic chip (PIC) with the chip's peripheral I/Os dedicated for electrical connection in the photonic package. Credit: *Journal of Optical Microsystems* (2024). DOI: 10.1117/1.JOM.4.1.011006

Photonics offers various advantages, including enablement of high-speed and low-loss communication by leveraging light properties in optical data communication, biomedical applications, automotive technology, and artificial intelligence domains. These advantages are realized

through complex photonic circuits, comprising diverse photonic elements that are integrated on a photonic chip.

Electronic chips are then added to supplement the photonic chips for certain functions, such as light source operation, modulation, and amplification. The close integration of electronic and photonic chips on a substrate is a critical aspect of photonic packaging.

Photonic packaging plays a vital role in supporting the effective operation of electronic and photonic chips across electrical, optical, mechanical, and thermal domains. Efficient thermal management becomes crucial in compact packages where thermal crosstalk between electronic and photonic chips, along with ambient temperature fluctuations, can negatively impact photonic chips' performance.

Glass substrates, widely discussed as a co-packaging platform for electronic and photonic chips are critical here because they offer advantages such as compact form factor, low electrical loss and a panel-level manufacturable platform. Additionally, glass substrates have low thermal conductivity, facilitating minimal lateral heat spreading between electronic and photonic chips.

The incorporation of through glass vias (TGVs) in glass substrate allows effective heat dissipation from electronic chips. Another thermal management strategy involves integrating micro-thermoelectric coolers (micro-TECs) on the underneath of a chip, providing active temperature control.

In new research published in the *Journal of Optical Microsystems*, a combination of TGVs and micro-TEC technologies termed "substrate integrated micro-thermoelectric coolers (SimTEC)" are introduced.

SimTEC involves TGVs partially filled with copper and thermoelectric

materials, ensuring thermal stabilization of photonic and electronic chips in the package. This novel technique complements system-level cooling approaches. Researcher Parnika Gupta and colleagues at University College Cork, Ireland, examined the impact of glass substrates on the thermal performance of segmented vias and compared it to that of the free-standing micro-TEC pillars. They analyzed the effect of via diameter, height, pitch, and fill-factor on SimTEC's cooling performance.

Notably, the technology provides precise thermal control in the package and reduces thermal resistance between the TEC surface and the chip interface when chips are flip-chip bonded on the glass substrate. Simulations with design of experiments (DOE) indicate a maximum cooling of 9.3 K or a temperature stabilization range of 18.6 K.

The study also underscored a six-times greater variation in cooling performance with the variation in via geometry as compared to the cooling performance variation of the free-standing micro-TEC unicouple. Optimizing thermoelectric material properties holds the potential for enhancing the performance of future SimTEC-integrated architectures.

More information: Parnika Gupta et al, Substrate integrated micro-thermoelectric coolers in glass substrate for next-generation photonic packages, *Journal of Optical Microsystems* (2024). DOI: 10.1117/1.JOM.4.1.011006

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