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Research investigates thermal impact of 3D stacking photonic and electronic chips

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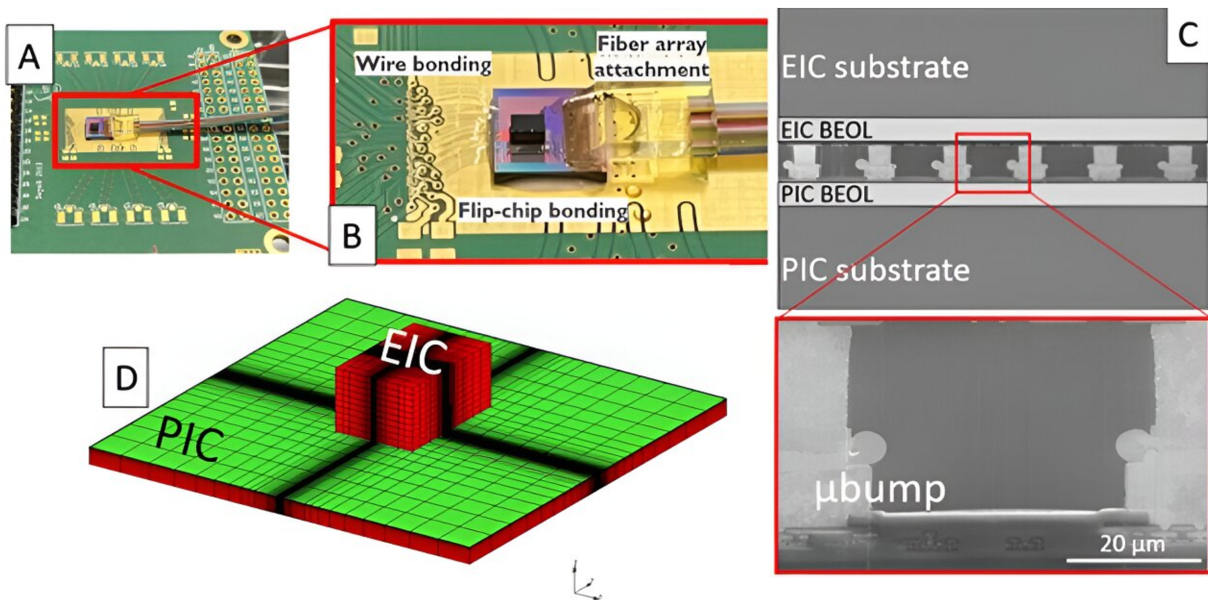

Hybrid, 3D integrated optical transceiver. (A,B) The test setup: the photonic chip (PIC) is placed on a circuit board (green), and the electronic chip (EIC) is bonded on top of the photonic chip. (C) is a cross-section of the EIC-PIC assembly with µbumps. (D) Shows the mesh of the finite element model. Credit: The Authors, doi: 10.1117/1.JOM.4.1.011004.

Recent advancements in AI and more specifically large language models such as ChatGPT have put a strain on data centers. AI models require huge amounts of data to train, and in order to move data between the processing units and memory, efficient communication links become

necessary.

For long-distance communication, fiber optics has already been the go-to solution for decades. For short-distance intra-data center communication, the industry is now also starting to adopt fiber optics due to its great performance compared to classical electrical links. Recent technological developments now even enable the switch from electrical to optical interconnect for very small distances, such as the communication between chips inside the same package.

This requires a conversion of the data stream from the electrical to the optical domain, which happens in the optical transceiver. Silicon photonics is the most widely used technology for fabricating these optical transceivers.

The active photonic devices inside the chip (modulators and photodetectors) still require a connection with electronic drivers for powering the devices and reading the incoming data. Stacking the electronic chip (EIC) right on top of the photonic chip (PIC) by means of 3D stacking technology realizes a very tight integration of the components with low parasitic capacitance.

In research recently published in the *Journal of Optical Microsystems*, the thermal impact of this 3D integration is investigated.

The design of the photonic chip consists of an array of ring modulators, which are known for their temperature sensitivity. To operate in a demanding environment, such as a data center, they need active thermal stabilization. This is implemented in the form of integrated heaters. For energy efficiency reasons, it is evident that the power required for thermal stabilization should be minimized.

The research team from KU Leuven and Imec in Belgium measured the

heater efficiency of the ring modulators experimentally before and after the flip-chip bonding of the EIC on the PIC. A relative loss of -43.3% in efficiency was found, which is a significant impact.

Furthermore, 3D finite element simulations attributed this loss to heat spreading in the EIC. This heat spreading should be avoided because, in the ideal case, all heat that is generated in the integrated heater is contained close to the photonic device. The thermal crosstalk between the photonic devices also increased by up to +44.4% after bonding the EIC, complicating the individual thermal control.

Quantifying the thermal impact of 3D photonic-electronic integration is essential, but so is the prevention of heater efficiency loss. For this reason, a thermal simulation study was conducted where typical design variables were changed with the goal of increasing the heater efficiency. It is shown that by increasing the spacing between µbumps and the photonic device and by decreasing the interconnect linewidth, the thermal penalty of 3D integration can be minimized.

More information: David Coenen et al, Thermal modeling of hybrid three-dimensional integrated, ring-based silicon photonic–electronic transceivers, *Journal of Optical Microsystems* (2023). DOI: 10.1117/1.JOM.4.1.011004

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