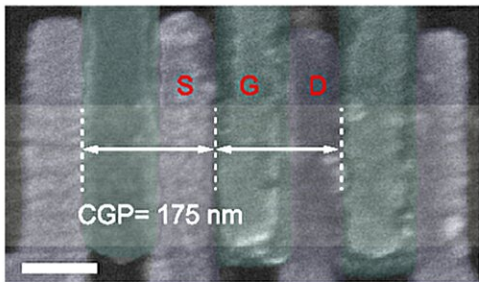


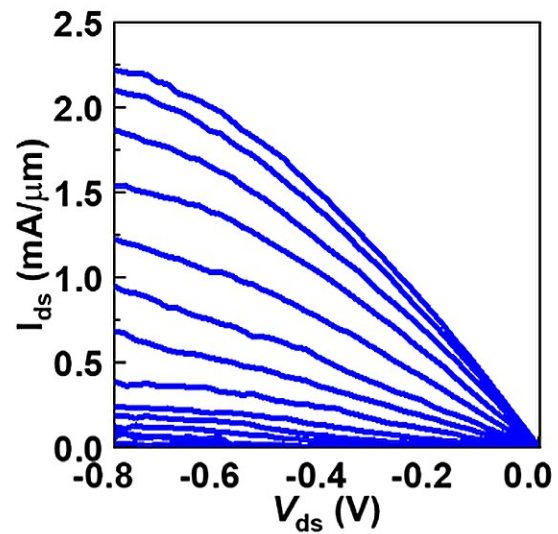
Researchers demonstrate scaling of aligned carbon nanotube transistors to below sub-10 nm nodes

July 27 2023, by Ingrid Fadelli

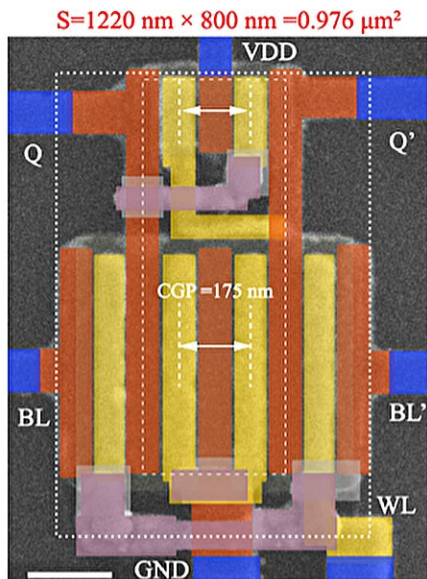
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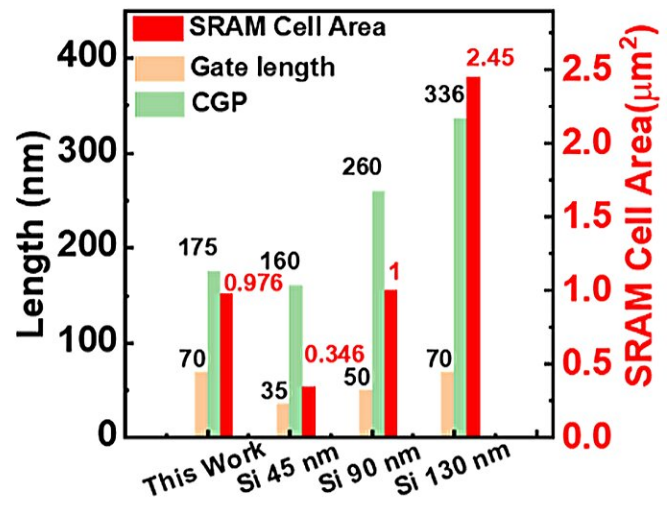
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90 nm node carbon nanotube technology. a, Carbon nanotube transistors based on nanotube arrays with contacted gate pitch of 175 nm. b, Output characteristics of the carbon nanotube transistors with contacted gate pitch of 175 nm. c, False-color SEM image of a representative 6T-SRAM cell with a contacted gate pitch of 175 nm and an area of $0.976 \mu\text{m}^2$. Scale bar 200 nm. d, Benchmarking the ultrascaled A-CNT 6T-SRAM cell with silicon 130 nm, 90 nm and 45 nm technology nodes for gate length, contacted gate pitch (CGP) and SRAM cell area. Credit: Lin et al

Carbon nanotubes, large cylindrical molecules composed of hybridized carbon atoms arranged in a hexagonal structure, recently attracted significant attention among electronics engineers. Due to their geometric configuration and advantageous electronic properties, these unique molecules could be used to create smaller field-effect transistors (FETs) that exhibit high energy efficiencies.

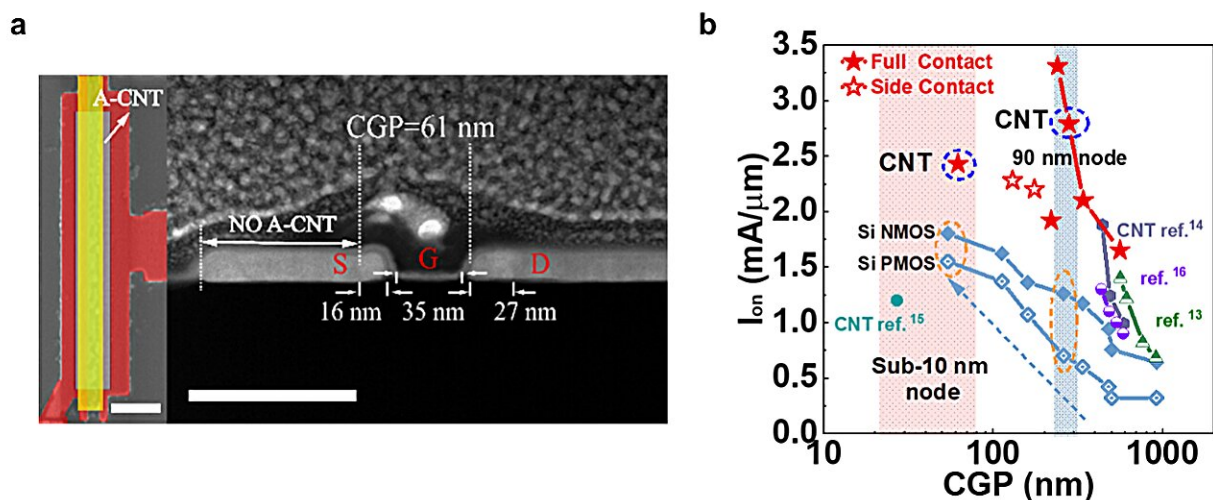
FETs based on carbon nanotubes have the potential to outperform smaller transistors based on silicon, yet their advantage in real-world implementations has yet to be conclusively demonstrated. A recent paper by researchers at Peking University and other institutes in China, published in *Nature Electronics*, outlines the realization of FETs based on carbon nanotubes that can be scaled to the same size of a 10 nm silicon technology node.

"Recent progress in achieving wafer-scale high density semiconducting carbon nanotube arrays brought us one step closer to the practical use of carbon nanotubes in CMOS circuits," Zhiyong Zhang, one of the researchers who carried out the study, told Phys.org. "However, previous research efforts have mainly focused on the scaling of channel or gate length of carbon nanotube transistors while keeping large contact dimensions, which cannot be accepted for high density CMOS circuits in practical applications.

"Our primary objective of this work is to explore the true scaling capability of carbon nanotube arrays using two figures of merit in silicon industry, that is, contacted gate pitch and area of 6T SRAM cell, while maintaining the performance advantages."

Zhang and his colleagues essentially set out to demonstrate the practical value of carbon nanotube transistors, showing that they can outperform conventional silicon-based FETs with a comparable gate pitch and a 6T SRAM cell area. To achieve this, they first fabricated FETs based on carbon nanotube arrays with a contacted gate pitch of 175 nm. This gate pitch was realized by scaling the gate length and contact length to 85 nm and 80 nm, respectively.

"Remarkably, the transistors exhibited an impressive on-current of 2.24 mA/μm and a peak transconductance of 1.64 mS/μm, surpassing the electronic performance of silicon 45 nm node transistors," Zhang said. "In addition, 6T SRAM cell consisted of these ultra-scaled nanotube transistors has been fabricated within 1 μm², and functions correctly. We then investigated the major obstacle, that is, the contact resistance of carbon nanotube transistors for further scaling."



Sub-10 nm node carbon nanotube technology. a, SEM and cross-sectional TEM images of an ultrascaled carbon nanotube transistor with a contacted gate pitch of 61 nm, a gate length (L_g) of 35 nm and a L_{con} of 16 nm. Scale bar of the SEM image: 200 nm; of the TEM image: 100 nm. b, Comparison of Ion at various CGP for carbon nanotube FETs in this work with that for other reported aligned carbon nanotube FETs and silicon technology. Credit: Lin et al

Past studies have shown that when following a widespread contact scheme known as "side contact," [charge carriers](#) can only be injected from the surface of carbon nanotubes. This makes the resistance of the nanotubes' length dependent, restricting the extent to which they can be miniaturized.

To overcome this issue, Zhang and his colleagues introduced a new scheme that they refer to as "full contact." This scheme entails cutting both ends of carbon nanotubes before forming the contact, which in turn allows part of the carriers to be injected from these ends.

"This new contact scheme enables carbon nanotube transistors to be further downscaled to contacted gate pitch below 55 nm that corresponds to silicon 10 nm technology node, while outperforming 10 nm node silicon transistors due to high carrier mobility and Fermi velocity," Zhang said. "Our work experimentally demonstrated a true 90 nm node technology using carbon nanotubes, which could be made geometrically smaller and offer electronic performance outperforming silicon 90 nm node transistors."

This recent paper introduces a reliable approach to down-scale carbon nanotube transistors, without compromising their performance. So far, the team used their strategy to create a 90 nm node transistor, but by re-

designing the structure of contacts they feel these transistors could be shrunk below a sub-10 nm node.

In the future, the work by Zhang and his colleagues could contribute to the creation of increasingly smaller and efficient carbon nanotube-based transistors. This could have valuable implications for the development of electronics.

"The next challenge that we are now tackling is to scale down the contact geometry for carbon nanotube n-type transistors to constructing complete CMOS technology, which is the necessary building blocks for modern digital ICs," Zhang added.

"Currently, we use scandium for the contact of n-type carbon nanotube transistors. However, we are facing great difficulties as we scale down the contact length due to the oxidation of this low-work function metal. In addition, we are working to accurately characterize the interface quality between [carbon nanotube](#) arrays and high- κ dielectric, improving it to the level of silicon CMOS transistors to enhance gate controllability and reliability."

More information: Yanxia Lin et al, Scaling aligned carbon nanotube transistors to a sub-10 nm node, *Nature Electronics* (2023). [DOI: 10.1038/s41928-023-00983-3](https://doi.org/10.1038/s41928-023-00983-3)

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