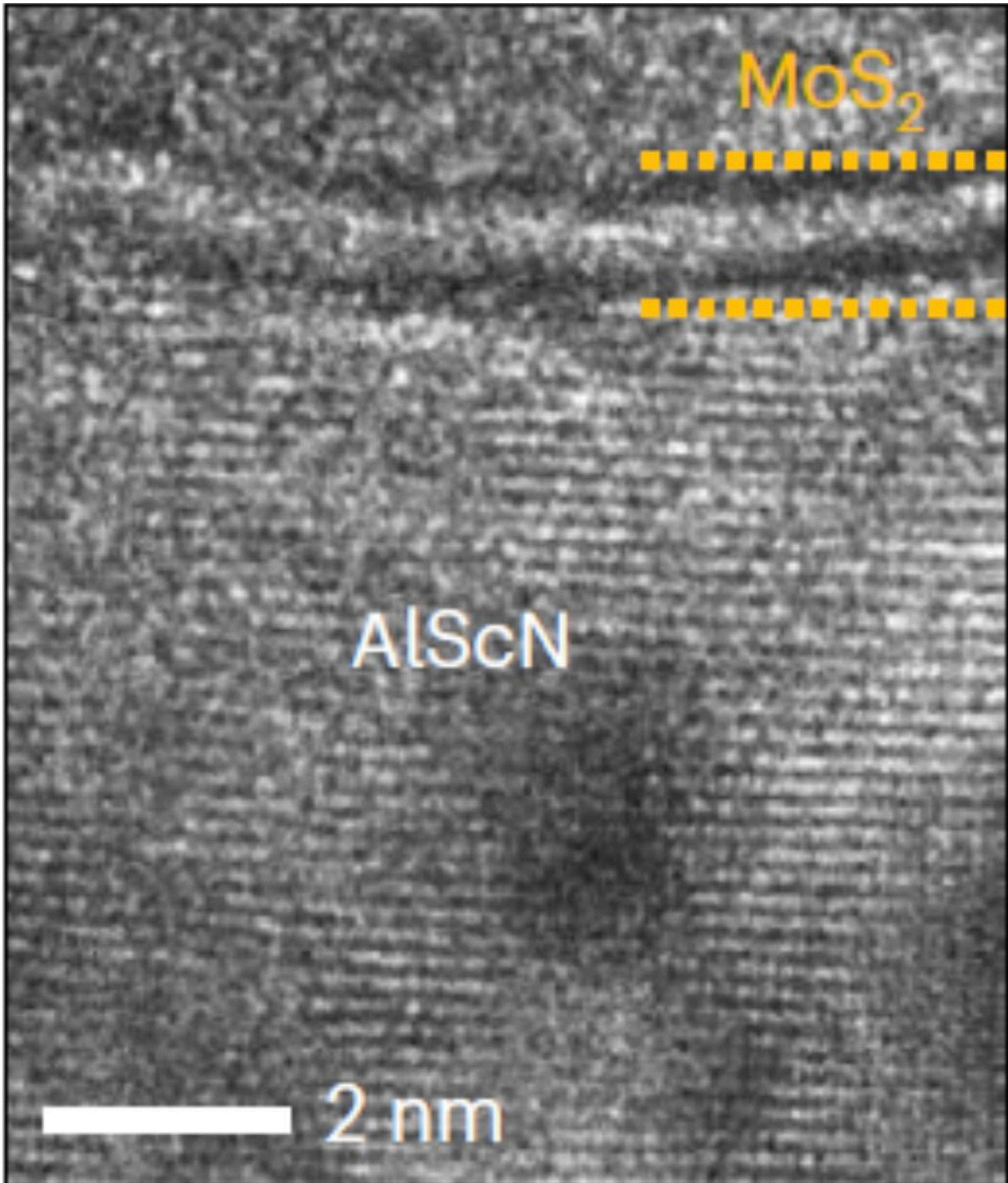
A scalable method to create ferroelectric FETs based on AlScN and 2D semiconductors

June 12 2023, by Ingrid Fadelli



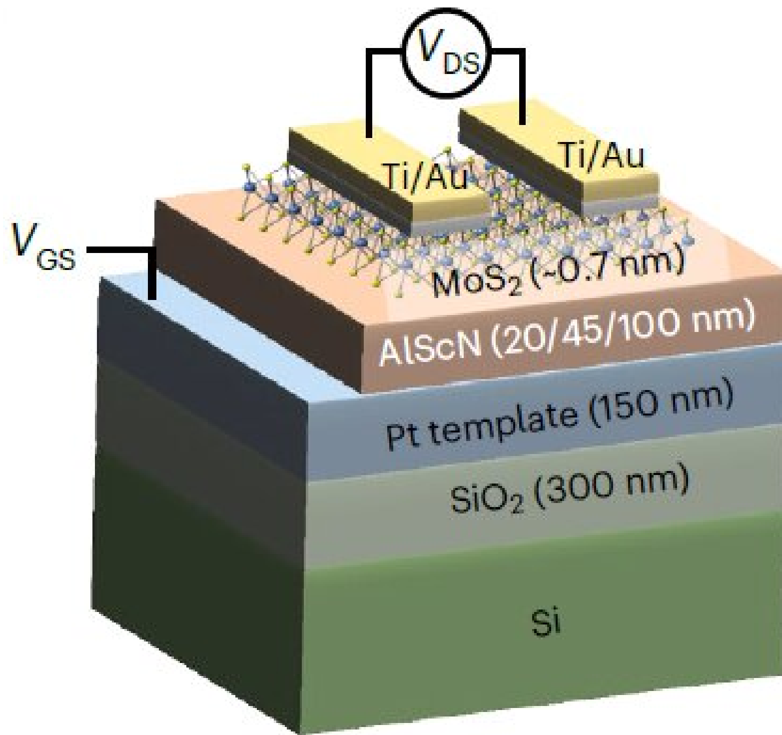
Phase-contrast lattice image of the MoS_2/ AlScN interface. Inset shows an electron diffraction pattern of the film stack on the zone axis of the Si (100) substrate. Credit: Kim et al

A key objective in the electronics engineering field is to develop transistors and other electronic components that are increasingly compact and efficient, utilizing readily available processes and materials. Among the transistors that have been found to be particularly promising are ferroelectric field effect transistors (FE-FETs), which resemble conventional FETs but also include ferroelectric materials.

FE-FETs contain gate insulators made of ferroelectric materials that can both switch and store electrical charge. In addition to regulating the current flow in electronic devices like conventional FETs, therefore, these ferroelectric-based transistors could also serve as memory devices.

This dual function could be highly advantageous for computationally demanding applications, such as running artificial intelligence (AI) models, as it could allow devices to better support their operation without consuming too much power. Despite their potential, FE-FETs have not yet been introduced on a large-scale, partly because reliably fabricating them on a large-scale using existing processes has proved to be challenging.

Researchers at University of Pennsylvania, Penn State University, and other universities worldwide recently introduced a strategy to create FE-FETs using similar processes to those currently employed to produce FETs. Their paper, published in *Nature Nanotechnology*, could pave the way toward the widespread adoption of these dual-function transistors.



Schematic of a MoS_2/AlScN FE-FET. Credit: Kim et al

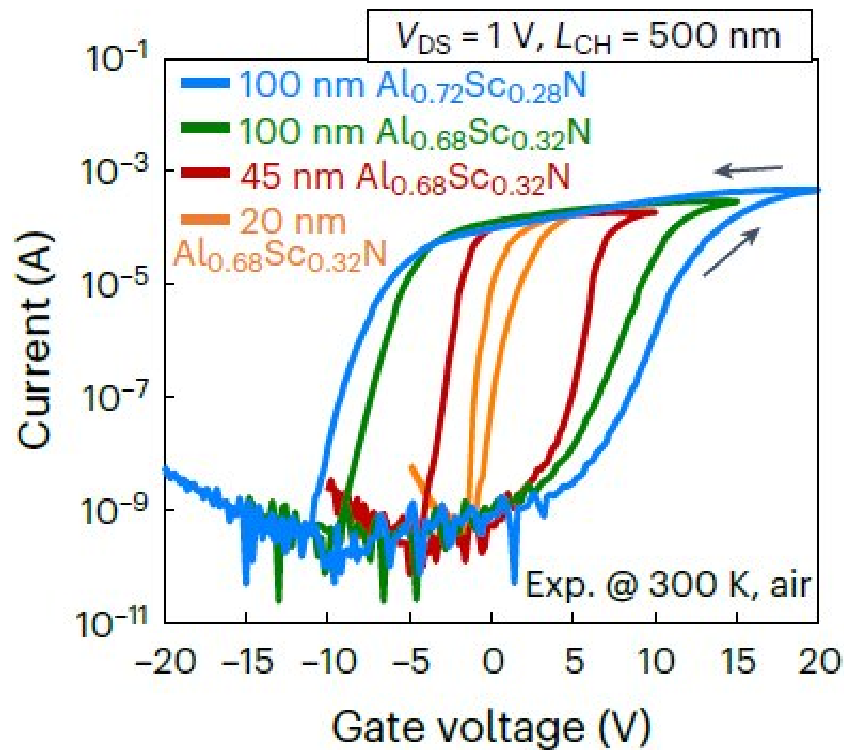
"The main motivation behind our study was to demonstrate that both 2D semiconductor materials such as MoS_2 and nitride ferroelectrics like AlScN (i.e., aluminum scandium nitride) are very attractive for realizing compact, low-power and fast non-volatile memory devices that can be directly integrated on Si CMOS technology in a back end of line (BEOL) process," Deep Jariwala, one of the researchers who carried out the study, told Phys.org. "We have been looking at 2D materials and AlScN for this application for some time now. Our present paper is a tour de force demonstration of materials scaled up to large areas and devices scaled down to very small dimensions and operating voltages."

Due to their ability to store and switch electrical charge almost indefinitely, even when a voltage applied at their gate electron is removed, FE-FETs could also act as non-volatile memory devices. The

primary goal of the study by Jariwala and his colleagues was to prove that FE-FETs can successfully be integrated with silicon semiconductor materials and could thus be fabricated to support the high bandwidth memory demands of big data applications.

"The charge stored by FE-FETs also modulates the conductivity of the 2D semiconductor into a high or low resistance state which actually represents the information stored in the memory device," Jariwala explained. "The key advantage of our strategy lies in the combination of AlScN ferroelectric material which has superlative ferroelectric properties and can be deposited in BEOL compatible processes and 2D semiconductors, which by virtue of their thin nature and van der Waals structure can allow strong modulation of the conductivity and can also be integrated with relative ease."

The FE-FETs created by the researchers integrate channels made of a 2D semiconductor with a ferroelectric material called AlScN, both of which were grown using conventional, wafer-scalable processes. The team tested a large array of their FE-FETs in a series of tests and found that they performed remarkably well, exhibiting memory windows larger than 7.8 V, ON/OFF ratios greater than 10^7 and ON-current density greater than 250 μA um^{-1} at ~80 nm channel length.



The transfer characteristics of the FE-FETs are recorded at 10 Hz rate with 0.2 V gate-voltage spacing. Credit: Kim et al

"Our demonstration proves that 2D semiconductor/AlScN FE-FET devices are ready for integration with Si CMOS to bring big-data computing requiring high bandwidth memory with processors in future generations of computer hardware," Jariwala said.

"Both these classes of materials are becoming mature, and our work creates a bridge for making this leap from the lab to the foundry, of these materials and memory devices."

The recent work by Jariwala and his colleagues could soon contribute to the large-scale implementation of FE-FETs. The prototypes they developed so far switch voltage at 3–4 volts, can store data well and could easily be integrated with some current silicon CMOS processors.

In their next studies, the researchers hope to reduce their size further, as this could facilitate their integration in consumer electronic devices.

"To truly see their advantage and performance gains in big data computing we will need to shrink these devices further," Jariwala added. "We are now working toward this, and as shown in another recent paper of ours, ferroelectric AlScN can be reliably made and switched at 5 nm thickness. Our next step will be to integrate 2D materials and make FE-FETs from 5 nm thick AlScN films to truly realize devices and achieve operation voltages that can be compatible with leading edge Si CMOS processors. At a FE-FET device level, we also need to do more work on improving metal/ 2D semiconductor contact resistance values and also make p-type FE-FET devices."

More information: Kwan-Ho Kim et al, Scalable CMOS back-end-of-line-compatible AlScN/two-dimensional channel ferroelectric field-effect transistors, *Nature Nanotechnology* (2023). DOI: 10.1038/s41565-023-01399-y

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