2D interfaces in future transistors may not be as flat as previously thought

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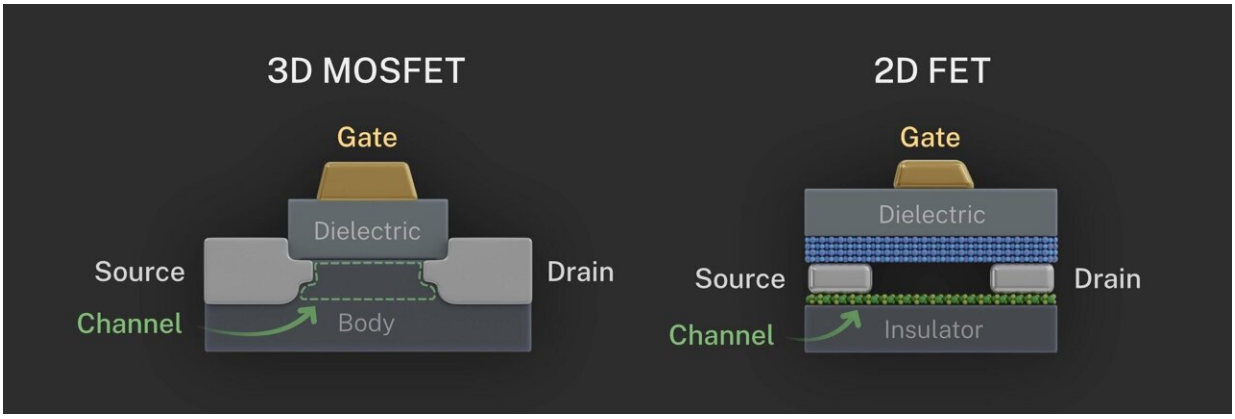


The general architecture of a traditional MOSFET vs. a 2D FET. A FET (field-effect transistor) is a device for regulating the flow of charge carriers (such as electrons) across a channel with three terminals: a source, a drain, and a gate. A MOSFET (metal oxide semiconductor field effect transistor) is by far the most widely used type of FET and is a building block of modern electronics, used in commercial electronic devices for more than 50 years. One main difference between the traditional 3D MOSFET and the "emerging technology" of the 2D FET is that the channel in a traditional MOSFET is in a 3D material, while a 2D FET's channel is a 2D material. Credit: Sean Kelley/NIST

Transistors are the building blocks of modern electronics, used in everything from televisions to laptops. As transistors have gotten smaller and more compact, so have electronics, which is why your cell phone is a super powerful computer that fits in the palm of your hand.

But there's a scaling problem: Transistors are now so small that they are difficult to turn off. A key device element is the channel that charge carriers (such as electrons) travel across between electrodes. If that channel gets too short, quantum effects allow electrons to effectively jump from one side to another even when they shouldn't.

One way to get past this sizing roadblock is to use layers of 2D materials—which are only a single atom thick—as the channel. Atomically thin channels can help enable even smaller transistors by making it harder for the electrons to jump between electrodes. One well-known example of a 2D material is graphene, whose discoverers won the Nobel Prize in Physics in 2010. But there are other 2D materials, and many believe they are the future of transistors, with the promise of scaling channel thickness down from its current 3D limit of a few nanometers (nm, billionths of a meter) to less than a single nanometer thickness.

Though research has exploded in this area, one issue has been persistently overlooked, according to a team of scientists from the National Institute of Standards and Technology (NIST), Purdue University, Duke University, and North Carolina State University. The 2D materials and their interfaces—which researchers intend to be flat when stacked on top of each other—may not, in fact, be flat. This non-flatness in turn can significantly affect device performance, sometimes in good ways and sometimes in bad.

In a new study published in the April 26, 2022, issue of *ACS Nano*, the research team reports the results of their measurements of the flatness of these interfaces in transistor devices that incorporate 2D materials. They are the first group to take high-resolution microscopy images showing flatness of these 2D layers in complete device arrays, on a relatively large scale—about 12 micrometers (millionths of a meter) as opposed to the more common 10-nm to 100-nm range.

Scientists successfully imaged a series of 2D-2D and 2D-3D interfaces in devices they created by using a variety of common fabrication methods. Their results show that assuming interfaces are flat when they are not is a much bigger issue than researchers in the field might have realized.

"We are enlightening the community to a problem that has been overlooked," said NIST's Curt Richter. "It's holding back the adoption of the new materials. The first step to solving the problem is knowing you have a problem."

Potential benefits include giving the scientific community more control over the fabrication of their devices.

"A lack of understanding about 2D interface flatness is a major roadblock for improving devices based on 2D materials," said lead author Zhihui Cheng, of NIST and Purdue University at the time of publication. "We've put out a method to quantify flatness to angstrom resolution. This opens a lot of windows for people to explore the strain and interactions at the 2D interfaces."

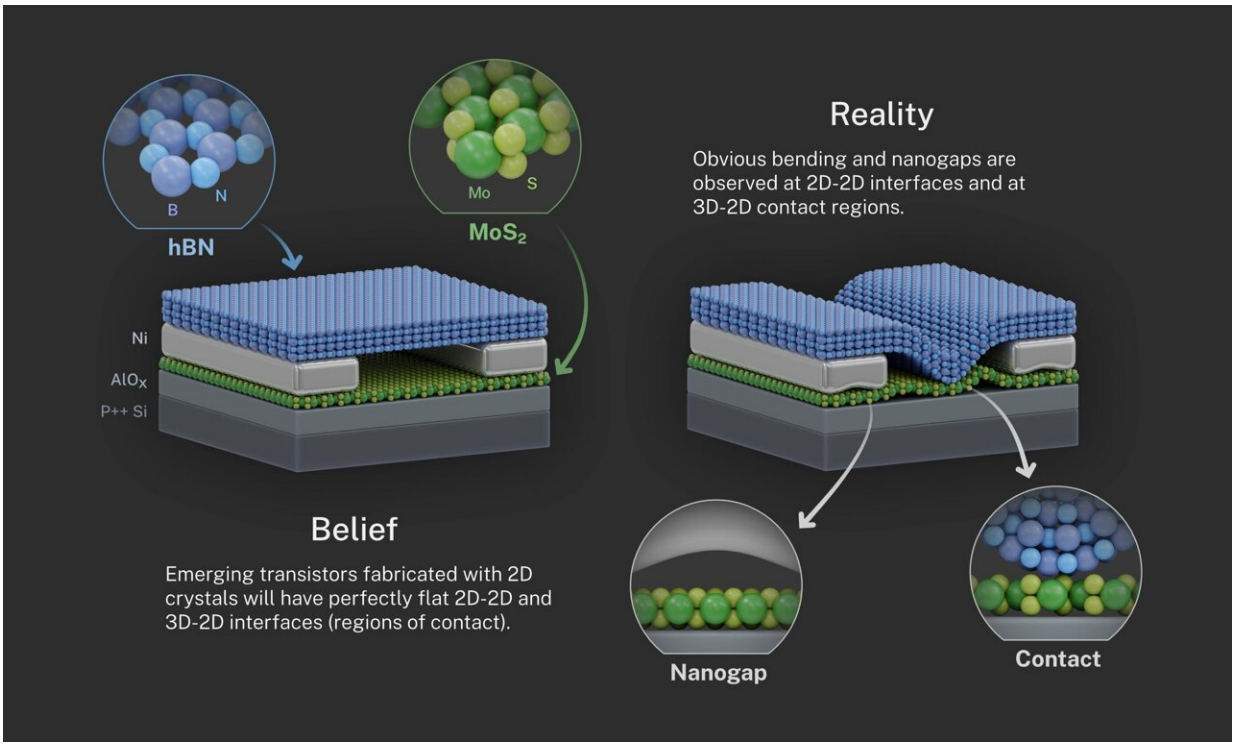
Not as flat as you think

In a traditional transistor, a 3D source electrode releases electrons across a 3D channel to a 3D drain electrode. In 2D transistors, electrons travel across a 2D material. The areas where these different materials meet are called interfaces.

A lack of flatness at these interfaces can cause problems with current flow in devices that use 2D materials. For example, if there is intimate physical contact between the source metal and the 2D channel, then there will also be intimate electrical contact and current will flow smoothly. Conversely, gaps between the 2D channel material and the

source compromise the electrical contact, which reduces current flow.

In their paper, the researchers explore several different types of 2D interfaces, including those made between nickel source and drain electrodes, a 2D channel made from the 2D crystal molybdenum disulfide (MoS_2), an encapsulating layer of the crystal hexagonal boron nitride (hBN), and aluminum oxide.



Researchers generally expect that transistors fabricated with 2D crystals will have perfectly flat 2D-2D and 3D-2D interfaces (regions of contact). But new evidence shows that in reality, there are obvious bending and nanogaps at these interfaces. Credit: Sean Kelley/NIST

Scientists typically put the 2D and 3D materials on top of each other

during the device fabrication process. For example, researchers sometimes stack 2D materials onto pre-patterned metal contacts. But the research team found that this kind of stacking of 2D materials had a profound effect on their flatness, particularly near the contact region. Adding hBN caused the MoS_2 to deform as high as 10 nm on one side of the contact. Areas further from the contacts tended to be relatively flat, though some of these areas still had a 2- to 3-nm gap.

While testing the effects of atomic layer deposition (a common technique used to lay down a thin layer of material) on 2D interface flatness, the research team found that a direct interface between aluminum oxide and MoS_2 is more deformed than the interfaces between hBN and MoS_2. When investigating the flatness of the 3D-2D contact interface, the team found surprisingly large nanocavities forming in the interface between the nickel contacts and the 2D MoS_2 channel.

To connect these non-flat interfaces back to real-world concerns about device performance, the team tested the electrical characteristics of a transistor made from these materials. Researchers found that the added non-flatness in the channel had the effect of actually improving the device performance.

"Overall, these results reveal how much the structure of 2D-2D and 2D-3D interfaces depends on the materials as well as the fabrication process," Cheng said.

To make its observations, the group used a type of high-resolution scanning transmission electron microscopy (scanning TEM), capable of resolving the images to the level of single atoms.

"So much of this field is pure research," Richter said. "People will make one device or maybe two, and they don't have extras that they can give to a microscopist to tear apart." In this study, on the other hand, the whole

point was to make the devices and then analyze them.

"We didn't do anything super special with the measurements," Richter continued. "But the combination of the electrical measurement know-how and the high-res TEM expertise—that's not a common thing."

"With the sub-angstrom resolution and record length in cross-sectional TEM, plus the correlation with device characteristics, our work has expanded and deepened the viewpoints on the complexity and intricacy of 2D interfaces," Cheng said.

With benefits to all

Applications of the work include reducing unintended device-to-device variation, of which 2D flatness is a significant contributing factor, the researchers said.

The imaging method could also ultimately help give scientists more control over fabrication. Certain processes introduce mechanical strain into the 2D structures, twisting them like a wrung-out washcloth or squishing and stretching them like an accordion. This can change the performance of a device in unpredictable ways that scientists don't yet fully understand. A better understanding of how strain affects device performance can give researchers more control over this performance.

"Strain is not always a bad thing," Richter said. "The high-end transistors people make today actually have built-in strain to make them work better. With the 2D materials it's not as obvious how to do that, but it may be possible to use non-flatness to create the strain you want."

The authors hope their work will inspire new efforts to increase the resolution of flatness measurements for 2D interfaces, even to sub-angstrom resolution.

"We have some preliminary data, but it's really just the beginning of this investigation," Cheng said.

More information: Zhihui Cheng et al, Are 2D Interfaces Really Flat?, *ACS Nano* (2022). DOI: 10.1021/acsnano.1c11493

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