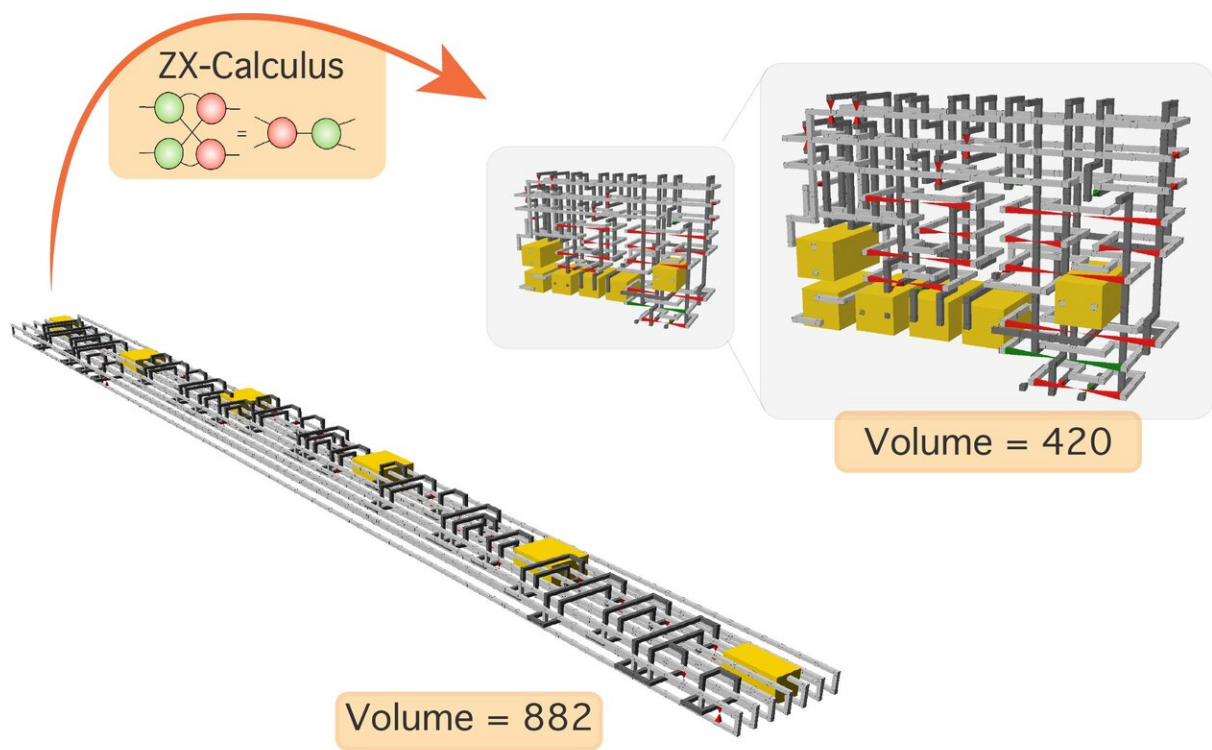# New approach to circuit compression could deliver real-world quantum computers years ahead of schedule

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Compression of a circuit that has an initial volume of 882 using the proposed method. The reduced circuit has a volume of 420, less than half its original volume. Credit: National Institute of Informatics

A major technical challenge for any practical, real-world quantum

computer comes from the need for a large number of physical qubits to deal with errors that accumulate during computation. Such quantum error correction is resource-intensive and computationally time-consuming. But researchers have found an effective software method that enables significant compression of quantum circuits, relaxing the demands placed on hardware development.

Quantum computers may still be far from a commercial reality, but what is termed 'quantum advantage'—the ability of a quantum computer to compute hundreds or thousands of times faster than a classical computer-has indeed been achieved on what are called Noisy Intermediate-Scale Quantum (NISQ) devices in early proof-of-principle experiments.

Unfortunately, NISQ devices are still prone to lots of errors that accumulate during their operation. For there to be any real-world application of quantum advantage, the design of a fully operational large-scale quantum computer with high error tolerance is required. Currently, NISQ devices can be engineered with approximately 100 qubits, but fault-tolerant computers would need millions of physical qubits at the very least to encode the logical information with sufficiently low error rates. A fault-tolerant implementation of quantum computational circuits not only makes the quantum computer larger, but also the runtime longer by orders of magnitude. An extended runtime itself in turn means the computation is even more susceptible to errors.

While advances in hardware may address this resource gap, researchers from the National Institute of Informatics (NII) and Nippon Telegraph and Telephone Corporation (NTT) in Japan tackled the problem from the software development side by compressing quantum circuits in large-scale fault-tolerant quantum computers, potentially reducing the need for hardware improvements.

"By compressing quantum circuits, we could reduce the size of the

quantum computer and its runtime, which in turn lessens the requirement for error protection," said Michael Hanks, a researcher at NII and one of the authors of a paper, published November 11 in *Physical Review X*.

Large-scale quantum computer architectures depend on an error correction code to function properly, the most commonly used of which is surface code and its variants.

The researchers focused on the circuit compression of one of these variants: the 3-D-topological code. This code behaves particularly well for distributed quantum computer approaches and has wide applicability to different varieties of hardware. In the 3-D-topological code, quantum circuits look like interlacing tubes or pipes, and are commonly called "braided circuits. The 3-D diagrams of braided circuits can be manipulated to compress and thus reduce the volume they occupy. Until now, the challenge has been that such "pipe manipulation" is performed in an ad-hoc fashion. Moreover, there have only been partial rules for how to do this.

"Previous compression approaches cannot guarantee whether the resulting quantum circuit is correct," said co-author Marta Estarellas, a researcher at NII. "One has to be very careful to check its correctness every time one of these compression rules is applied. This is an important issue, as such a task is as hard as running the whole quantum circuit."

The research team proposes the use of ZX-calculus as a language for this intermediate stage of compilation. ZX-calculus is a 2-D diagrammatic language (using diagrams and imagery instead of words) developed in the late 2000s expressly to allow an intuitive representation of qubit processes. More importantly, it comes with a complete set of manipulation rules.

In their paper, the researchers harness ZX-calculus by discovering the translation relations between ZX-calculus and the components of the braided circuit. The researchers have shown that these two representations of logical gate circuits can be mapped to one another by identifying a new interpretation that had been hidden within ZX-calculus all along.

The ZX-calculus language can apply a set of transformation rules to alter the structure of the circuit without altering its underlying mathematical meaning (and thus its operation) and therefore ensuring its correctness. By altering that conceptual structure carefully, the volume of the circuit can be minimized, achieving considerable compression rates once this new structure is mapped to the actual braided quantum circuit.

Applying this technique, the researchers report compression reductions of up to 77 percent, equivalent to a 40 percent reduction compared to the best previous efforts.

"The compression method and its further development could deliver realization of a real-world fault-tolerant quantum computer years ahead of schedule," said William J. Munro, a research scientist at NTT, who also contributed to the research.

"Interestingly, it could also be the foundation of future operating system development," said Kae Nemoto, Director of the Global Research Center for Quantum Information Science at NII. "It could still take many years for these software developments to be implemented in fully-scalable quantum computers, but our method could save a great deal of effort associated with hardware development in the meantime."

More information: Michael Hanks et al, Effective Compression of Quantum Braided Circuits Aided by ZX-Calculus, *Physical Review X* (2020). DOI: 10.1103/PhysRevX.10.041030