Examining trapped ion technology for next generation quantum computers

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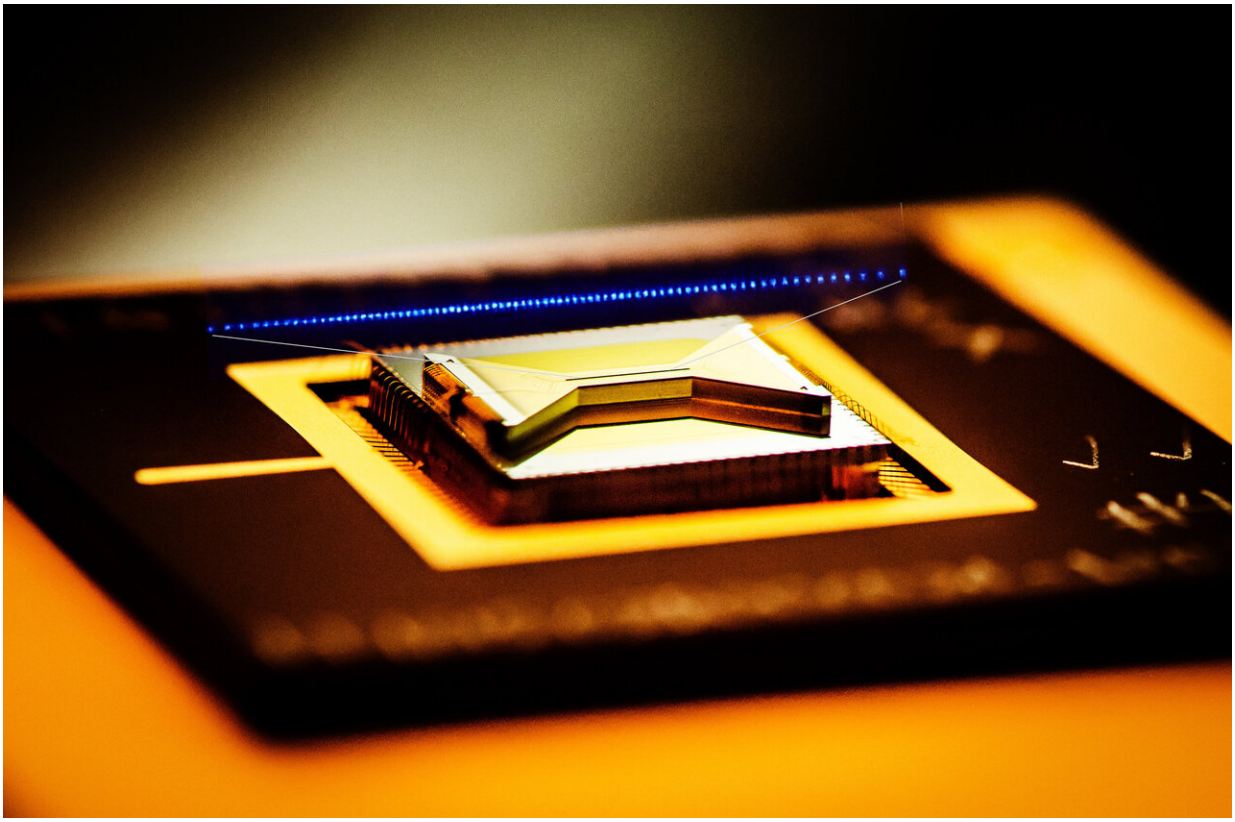

IonQ's trapped ion system. Credit: Duke University, staq.pratt.duke.edu/

Quantum computers (QC) are poised to drive important advances in several domains, including medicine, material science and internet security. While current QC systems are small, several industry and

academic efforts are underway to build large systems with many hundred qubits.

Towards this, computer scientists at Princeton University and physicists from Duke University collaborated to develop methods to design the next generation of quantum computers. Their study focused on QC systems built using trapped ion (TI) technology, which is one of the current front-running QC hardware technologies. By bringing together computer architecture techniques and device simulations, the team showed that co-designing near-term hardware with applications can potentially improve the reliability of TI systems by up to four orders of magnitude.

Their study was conducted as a part of the Software-Tailored Architecture for Quantum co-design (STAQ) project, an NSF funded collaborative research effort to build an trapped-ion quantum computer and the NSF CISE Expedition in Computing Enabling Practical-Scale Quantum Computing (EPiQC) project. It was published recently in the 2020 ACM/IEEE International Symposium on Computer Architecture.

Towards larger trapped-ion quantum computers

Trapped-ions (TI) are one of the leading candidates for building qubits (quantum bits). In a TI system, atomic ion qubits (like a Calcium or Ytterbium ion) are isolated and trapped in an electric field. To store quantum information, the internal atomic states of the ions are used to represent the 0 and 1 qubit states. By pulsing the ions using carefully tuned lasers, these systems can perform gates (instructions) on this information, leading to computations which can run much faster than on a standard "classical" computer. Companies such as IonQ, Honeywell, and Alpine Quantum Technologies, as well as academic groups like ours at Duke University, are working to build QC systems using such hardware. Published results on single ion chains include the complete

control of 11 qubits at IonQ and quantum simulations on 53 qubits at the University of Maryland.

While current TI devices have shown significant promise, larger devices with 50 to 100 qubits are necessary to demonstrate advantages over classical computing. However, most current TI devices have a fundamental scaling bottleneck—they are based on a monolithic single-trap architecture, where all ions are housed in the same trapping zone. In this architecture, qubit control and gate implementation become increasingly challenging as more ions are added to the trap.

Recognizing these difficulties, an alternative scalable architecture, called Quantum Charged Coupled Device (QCCD) was proposed as early as 2002. A QCCD system is composed of a set of traps, each holding a small number of ions, instead of a single large trap.

Similar to single-trap architectures, gates can be performed on one or more ions that are co-located within a trap. To enable entanglement across traps, QCCD uses ion shuttling to communicate ions across the system. That is, when a two-qubit operation is to be performed on a pair of ions which are in different traps, one of the ions is physically moved to the other trap, co-locating the ions before the gate is executed. Over the last two decades, all operations required for building these systems have been developed and honed. Recently, Honeywell integrated these components to build the first QCCD system having 4 qubits.

Architecting the next generation of QCCD systems

To build the next generation of QCCD systems with 50 to 100 qubits, hardware designers have to tackle a variety of conflicting design choices. "How many ions should we place in each trap? What communication topologies work well for near-term QC applications? What are the best methods for implementing gates and shuttling operations in hardware?

These are key design questions that our work seeks to answer," said Prakash Murali, a graduate student at Princeton University. Although individual experiments have been performed to understand some of these choices, there are no studies on the impact of these choices on applications and their overall system-level performance and reliability tradeoffs. Furthermore, hardware designers have to contend with unreliable gates and other limitations of near-term systems and still support an evolving mix of quantum applications.

To study these design choices efficiently, the researchers built a design tool flow which estimates the reliability, execution time and other metrics for a set of quantum programs on a specified QCCD device. This tool flow consists of two parts. The first part is a compiler which maps the program down to the primitive operations that will be available on QCCD systems. Since shuttling is error-prone and time-consuming, the compiler seeks to improve the overall application reliability and performance by minimizing the total amount of shuttling. The second part is a QCCD simulator which uses realistic performance and noise models for QCCD systems, derived from hardware characterization works, to estimate the quality of an application execution. "Together, these components allow us to automatically characterize a large design space and test the impact of device architecture across applications," said Murali.

Using this tool flow, they identified a sweet spot of 15 to 25 ions per trap that will likely work well across applications, providing the best tradeoff between gate errors at high trap sizes and shuttling errors at low trap sizes. Overall, they showed that tuning the architectural attributes of the system such as the number of ions in a trap and topology can impact the reliability of application executions by as much as three orders of magnitude. Further, optimizing the low-level gate implementations and shuttling methods can further improve the reliability by another order of magnitude. "By understanding the way these different choices interact,

our work enables QCCD systems which can perform useful computations in the near term, before quantum computers are large enough to become truly reliable," said researcher Dripto Debroy, a graduate student at Duke University.

Computer architecture and simulation-based design have been a key enabler of technology progress in classical computing. By leveraging these techniques for QC design and adopting a full system-view of the design space, rather than focusing on hardware alone, this study seeks to accelerate the progress towards the next major milestone of 50 to100 qubits. Currently the two most promising ideas for scaling to 1000s of ions are large QCCD systems and photonic interconnects between small QCCD systems. This architectural study of near-term QCCD devices has the potential to guide QC hardware design for both future directions.

More information: Link to the paper mrmgroup.cs.princeton.edu/pape … s/pmurali-isca20.pdf

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