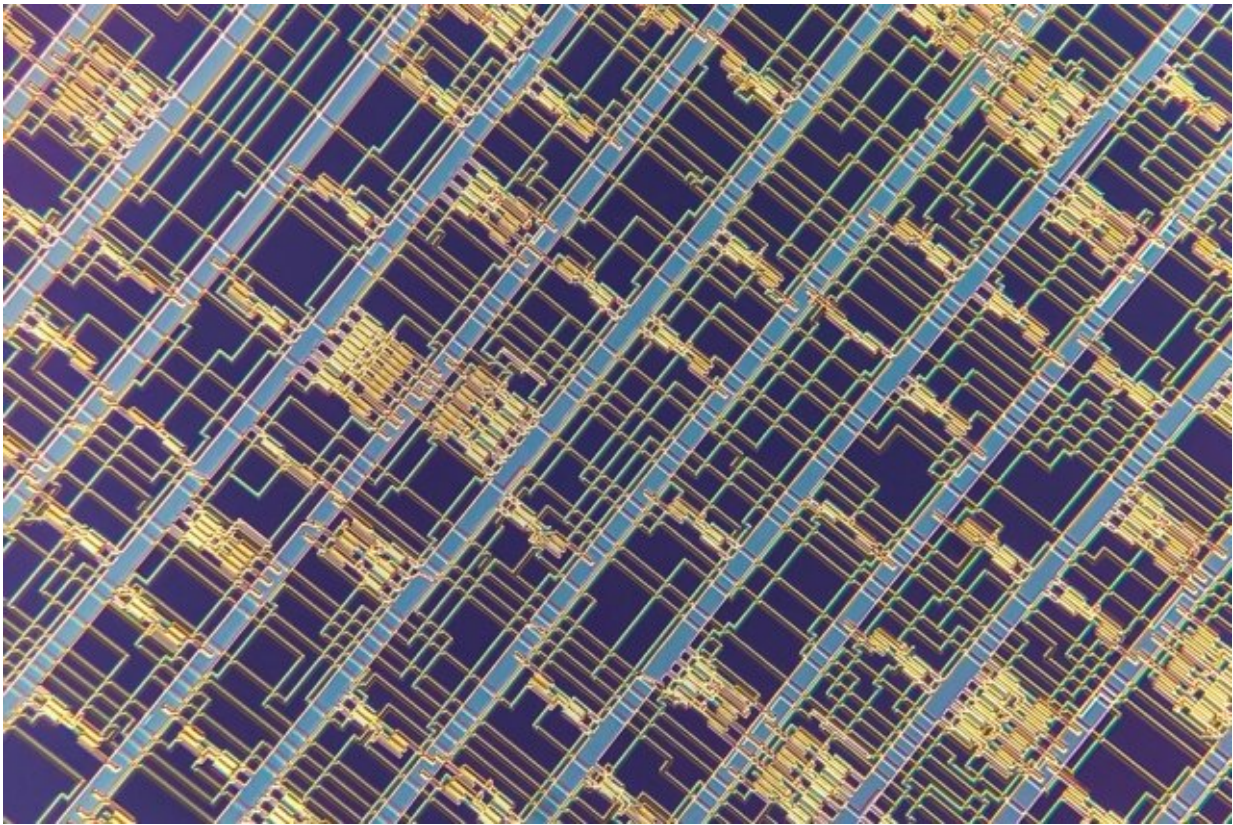


# Engineers build advanced microprocessor out of carbon nanotubes

August 29 2019, by Rob Matheson

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A close up of a modern microprocessor built from carbon nanotube field-effect transistors. Credit: Felice Frankel

After years of tackling numerous design and manufacturing challenges, MIT researchers have built a modern microprocessor from carbon

nanotube transistors, which are widely seen as a faster, greener alternative to their traditional silicon counterparts.

The microprocessor, described today in the journal *Nature*, can be built using traditional silicon-chip fabrication processes, representing a major step toward making [carbon](#) nanotube microprocessors more practical.

Silicon transistors—critical microprocessor components that switch between 1 and 0 bits to carry out computations—have carried the computer industry for decades. As predicted by Moore's Law, industry has been able to shrink down and cram more transistors onto chips every couple of years to help carry out increasingly complex computations. But experts now foresee a time when [silicon transistors](#) will stop shrinking, and become increasingly inefficient.

Making carbon nanotube field-effect transistors (CNFET) has become a major goal for building next-generation computers. Research indicates CNFETs have properties that promise around 10 times the energy efficiency and far greater speeds compared to silicon. But when fabricated at scale, the transistors often come with many defects that affect performance, so they remain impractical.

The MIT researchers have invented new techniques to dramatically limit defects and enable full functional control in fabricating CNFETs, using processes in traditional silicon chip foundries. They demonstrated a 16-bit microprocessor with more than 14,000 CNFETs that performs the same tasks as commercial microprocessors. The *Nature* paper describes the microprocessor design and includes more than 70 pages detailing the manufacturing methodology.

The microprocessor is based on the RISC-V open-source chip architecture that has a set of instructions that a microprocessor can execute. The researchers' microprocessor was able to execute the full set

of instructions accurately. It also executed a modified version of the classic "Hello, World!" program, printing out, "Hello, World! I am RV16XNano, made from CNTs."

"This is by far the most advanced chip made from any emerging nanotechnology that is promising for high-performance and energy-efficient computing," says co-author Max M. Shulaker, the Emanuel E Landsman Career Development Assistant Professor of Electrical Engineering and Computer Science (EECS) and a member of the Microsystems Technology Laboratories. "There are limits to silicon. If we want to continue to have gains in computing, carbon nanotubes represent one of the most promising ways to overcome those limits. [The paper] completely re-invents how we build chips with carbon nanotubes."

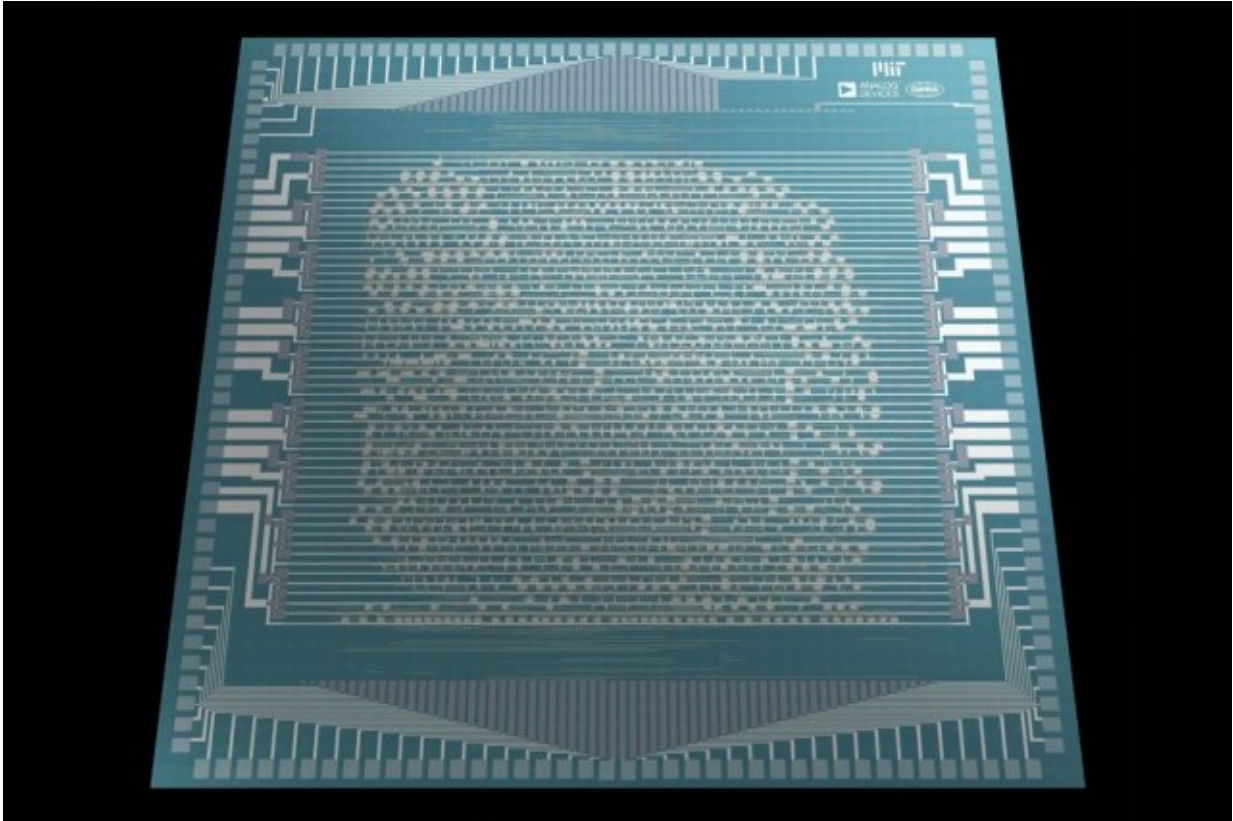
Joining Shulaker on the paper are: first author and postdoc Gage Hills, graduate students Christian Lau, Andrew Wright, Mindy D. Bishop, Tathagata Srimani, Pritpal Kanhaiya, Rebecca Ho, and Aya Amer, all of EECS; Arvind, the Johnson Professor of Computer Science and Engineering and a researcher in the Computer Science and Artificial Intelligence Laboratory; Anantha Chandrakasan, the dean of the School of Engineering and the Vannevar Bush Professor of Electrical Engineering and Computer Science; and Samuel Fuller, Yosi Stein, and Denis Murphy, all of Analog Devices.

## **Fighting the "bane" of CNFETs**

The microprocessor builds on a previous iteration designed by Shulaker and other researchers six years ago that had only 178 CNFETs and ran on a single bit of data. Since then, Shulaker and his MIT colleagues have tackled three specific challenges in producing the devices: material defects, manufacturing defects, and functional issues. Hills did the bulk of the microprocessor design, while Lau handled most of the



manufacturing.



MIT engineers have built a modern microprocessor from carbon nanotube field-effect transistors (pictured), which are seen as faster and greener than silicon transistors. The new approach uses the same fabrication processes used for silicon chips. Credit: Massachusetts Institute of Technology

For years, the defects intrinsic to carbon nanotubes have been a "bane of the field," Shulaker says. Ideally, CNFETs need semiconducting properties to switch their conductivity on an off, corresponding to the bits 1 and 0. But unavoidably, a small portion of carbon nanotubes will be metallic, and will slow or stop the transistor from switching. To be robust to those failures, advanced circuits will need carbon nanotubes at

around 99.999999 percent purity, which is virtually impossible to produce today.

The researchers came up with a technique called DREAM (an acronym for "designing resiliency against metallic CNTs"), which positions metallic CNFETs in a way that they won't disrupt computing. In doing so, they relaxed that stringent purity requirement by around four orders of magnitude—or 10,000 times—meaning they only need carbon nanotubes at about 99.99 percent purity, which is currently possible.

Designing circuits basically requires a library of different logic gates attached to transistors that can be combined to, say, create adders and multipliers—like combining letters in the alphabet to create words. The researchers realized that the metallic carbon nanotubes impacted different pairings of these gates differently. A single metallic carbon nanotube in gate A, for instance, may break the connection between A and B. But several metallic carbon nanotubes in gates B may not impact any of its connections.

In chip design, there are many ways to implement code onto a circuit. The researchers ran simulations to find all the different gate combinations that would be robust and wouldn't be robust to any metallic carbon nanotubes. They then customized a chip-design program to automatically learn the combinations least likely to be affected by metallic carbon nanotubes. When designing a new chip, the program will only utilize the robust combinations and ignore the vulnerable combinations.

"The 'DREAM' pun is very much intended, because it's the dream solution," Shulaker says. "This allows us to buy carbon nanotubes off the shelf, drop them onto a wafer, and just build our circuit like normal, without doing anything else special."

## Exfoliating and tuning

CNFET fabrication starts with depositing carbon nanotubes in a solution onto a wafer with predesigned transistor architectures. However, some carbon nanotubes inevitably stick randomly together to form big bundles—like strands of spaghetti formed into little balls—that form big particle contamination on the chip.

To cleanse that contamination, the researchers created RINSE (for "removal of incubated nanotubes through selective exfoliation"). The wafer gets pretreated with an agent that promotes [carbon nanotube](#) adhesion. Then, the wafer is coated with a certain polymer and dipped in a special solvent. That washes away the polymer, which only carries away the big bundles, while the single carbon nanotubes remain stuck to the wafer. The technique leads to about a 250-times reduction in particle density on the chip compared to similar methods.

Lastly, the researchers tackled common functional issues with CNFETs. Binary computing requires two types of transistors: "N" types, which turn on with a 1 bit and off with a 0 bit, and "P" types, which do the opposite. Traditionally, making the two types out of carbon nanotubes has been challenging, often yielding transistors that vary in performance. For this solution, the researchers developed a technique called MIXED (for "metal interface engineering crossed with electrostatic doping"), which precisely tunes transistors for function and optimization.

In this technique, they attach certain metals to each transistor—platinum or titanium—which allows them to fix that transistor as P or N. Then, they coat the CNFETs in an oxide compound through atomic-layer deposition, which allows them to tune the transistors' characteristics for specific applications. Servers, for instance, often require transistors that act very fast but use up energy and power. Wearables and medical implants, on the other hand, may use slower, low-power [transistors](#).

The main goal is to get the chips out into the real world. To that end, the researchers have now started implementing their manufacturing techniques into a silicon chip foundry through a program by Defense Advanced Research Projects Agency, which supported the research. Although no one can say when chips made entirely from carbon [nanotubes](#) will hit the shelves, Shulaker says it could be fewer than five years. "We think it's no longer a question of if, but when," he says.

**More information:** Gage Hills et al. Modern microprocessor built from complementary carbon nanotube transistors, *Nature* (2019). [DOI: 10.1038/s41586-019-1493-8](https://doi.org/10.1038/s41586-019-1493-8)

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