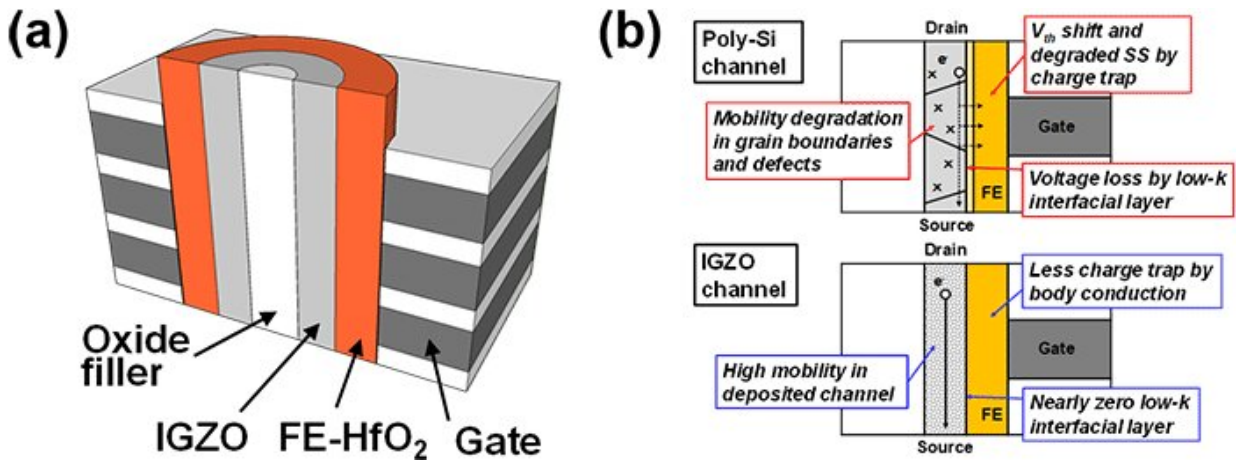
A device emerges from the fusion of IGZO and ferroelectric-HfO2

June 18 2019



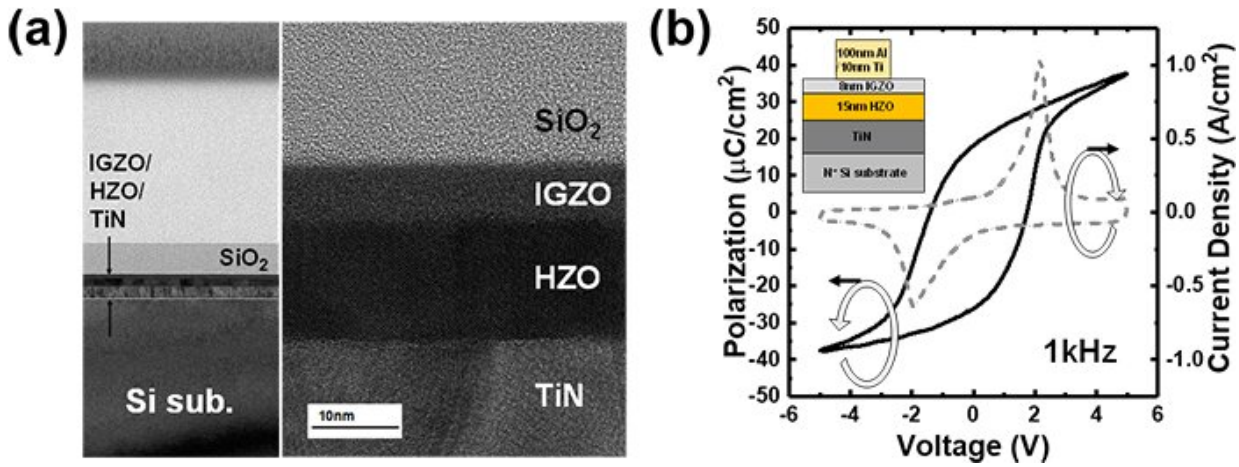
(a) Schematic of ferroelectric-HfO2 based FeFET with 3D vertical stack structure for high memory capacity. Poly-silicon is typically used as a channel material. In this work, we propose to use IGZO as a channel material. (b) Schematic illustration of current challenges of poly-silicon channel and possible solution by IGZO channel. Poly-silicon has low mobility in nanometer thickness region and forms low-k interfacial layer which causes voltage loss and charge trapping.

As a part of JST PRESTO program, Associate professor Masaharu Kobayashi, Institute of Industrial Science, the University of Tokyo, has developed a ferroelectric FET (FeFET) with ferroelectric-HfO_2 and ultrathin IGZO channel. Nearly ideal subthreshold swing (SS) and mobility higher than poly-silicon channel have been demonstrated.

FeFET is a promising memory device because of its low-power, high-speed and high-capacity. After the discovery of CMOS-compatible ferroelectric-HfO_2 material, FeFET has been attracting more attention. For even higher memory capacity, 3-D vertical stack structure has been proposed as shown in Fig. 1(a).

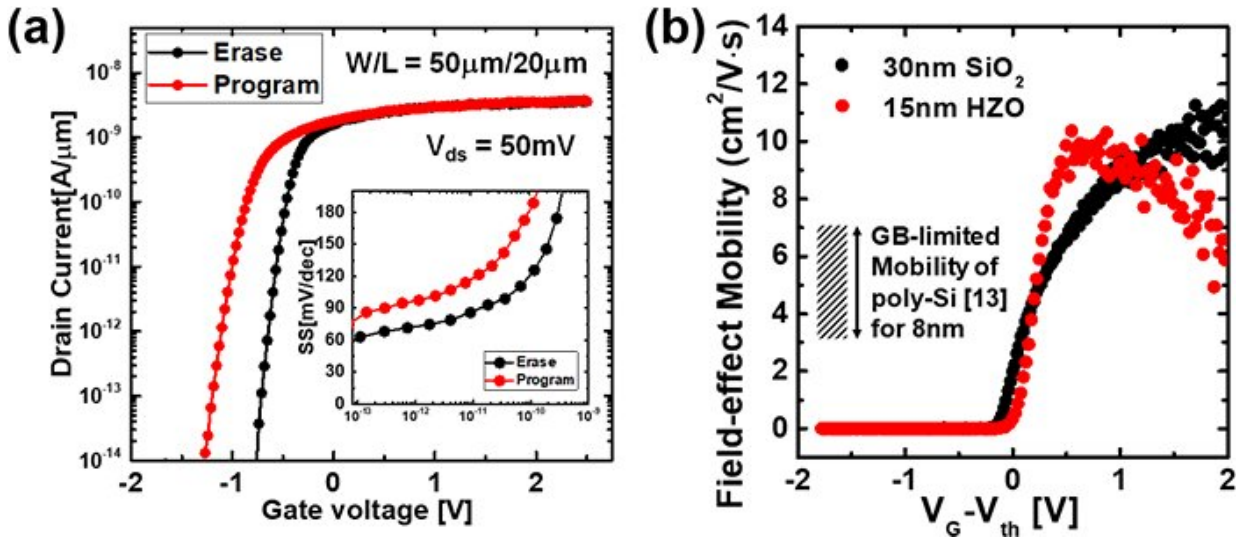
For 3-D vertical stack structure, poly-silicon is typically used as a channel material. However, poly-silicon has very low mobility in nanometer thickness region due to grain boundaries and extrinsic defects. Moreover, poly-silicon forms a low-k interfacial layer with ferroelectric-HfO_2 gate insulator. This results in voltage loss and charge trapping which prevents low voltage operation and degrades reliability, respectively as shown in Fig. 1(b).

To solve these problems, in this study, we proposed a ferroelectric-HfO_2 based FeFET with ultrathin IGZO channel. IGZO is a metal-oxide semiconductor and can avoid low-k interfacial layer with a ferroelectric HfO_2 gate insulator. Moreover, since IGZO is an N-type semiconductor and typically used in junctionless transistor operations, charge trapping, which is a serious problem in inversion mode operation, can be avoided as shown in Fig. 1(b).



(a) Cross-sectional TEM image of a TiN/HfZrO2/IGZO capacitor. Each layer was uniformly formed. HfZrO2 layer is uniformly crystallized having ferroelectric phase. (b) Measured polarization charge versus voltage of a TiN/HfZrO2/IGZO capacitor. Clear ferroelectricity was confirmed.

First, we systematically investigated optimum IGZO channel thickness. As IGZO thickness decreases, SS is reduced and threshold voltage (Vth) increases. To realize steep SS and normally-off operation, 8nm was chosen. Next, we fabricated an TiN/$HfZrO_2$/IGZO capacitor. $HfZrO_2$ is the ferroelectric layer. Cross-sectional TEM image shows that each layer was uniformly formed as shown in Fig. 2(a). GIXRD spectrum was taken and ferroelectric phase was confirmed. By electrical characterization, we confirmed clear ferroelectric property with IGZO capping on $HfZrO_2$ as shown in Fig. 2(b).



(a) Measured drain current versus gate voltage of an FeFET with 8nm-thick IGZO channel. Memory window of 0.5V and nearly ideal SS of 60mV/dec were

achieved. (b) Measured field-effect mobility of the FeFET with IGZO channel. Mobility of 10cm2/Vs can be higher than that of poly-silicon channel at the same thickness.

It should be noted that, in the current device design, a back-gate is needed with buried oxide to fix the body potential. Without a back-gate, body potential is floating and voltage cannot be sufficiently applied on the ferroelectric-HfO_2 gate insulator, which was confirmed by TCAD simulation. Based on these device designs, we fabricated a FeFET with ferroelectric-HfO_2 and an ultrathin IGZO channel. Fig. 3(a) shows the measured drain-current versus gate-voltage after applying write and erase pulse voltages. A 0.5V memory window and nearly ideal SS of 60mV/dec was obtained. In addition, field-effect mobility is about 10cm2/Vs as shown in Fig. 3(b), which can be higher than poly-silicon at the same thickness.

The achievements in this study will open a new path for realizing low-voltage and highly reliable FeFET with 3-D vertical stack structure. This leads to enabling ultralow power IoT edge devices, deploying highly sophisticated network system, and thus providing more strategic social services utilizing big data.

More information: Fei Mo et al. Experimental Demonstration of Ferroelectric HfO2 FET with Ultrathin-body IGZO for High-Density and Low-Power Memory Applicatione, VLSI Technology Symposium 2019, pp. 42-43.

Provided by Japan Science and Technology Agency