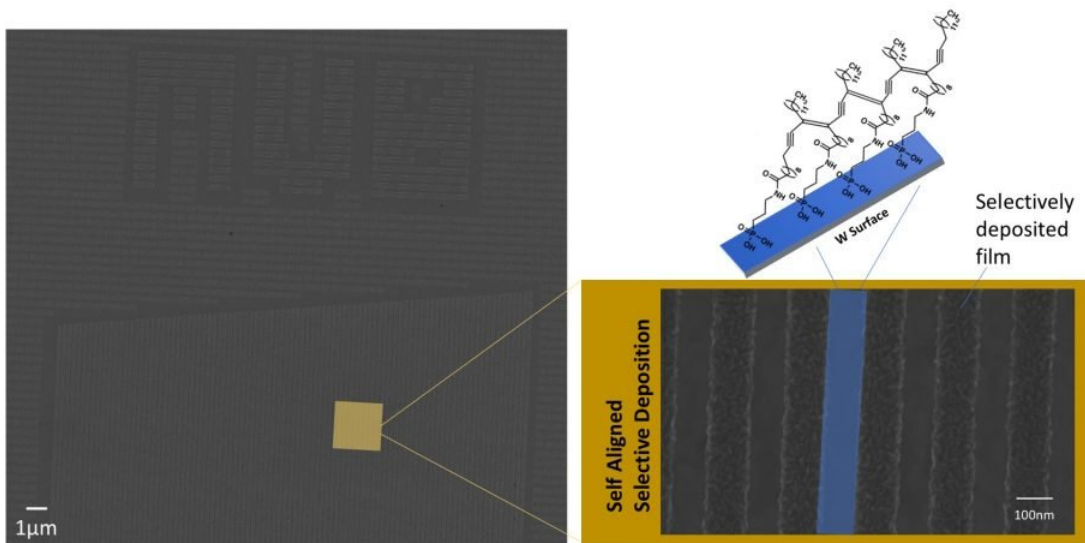


# Enabling fabrication beyond 7nm

November 19 2018, by Rudy J Wojtecki



Scanning Electron Micrograph of a large field region showing low defectivity in a selectively deposited film, highlighted region is a large area with 100nm line spaces. Inset, enlarged area of a prepatterned tungsten surface where highlighted (blue) areas contain an inhibitory molecule synthesized at IBM Research – Almaden. Credit: IBM

How did we get from the Palm Pilots of the 90s to the ultra-powerful smart phones of today? In large part, because of scaling, where integrated circuits are made with smaller feature sizes fitting more and more circuit elements in the same area of silicon at each technology

generation. This sets our expectations that in 20 more years, our mobile devices of today will look like the Palm Pilot of yesterday. However, as current semiconductor fabrication processes are nearing fundamental limits, and the emergence of AI is driving demand for non-traditional computing architectures, new methods to fabricate at the nanoscale are required.

My team at IBM Research – Almaden in Silicon Valley has invented several [new materials](#) and material science processes that help address these issues. Our work, published recently in *Applied Materials & Interfaces*, shows a [method](#) of selectively depositing a material on feature sizes as small as 15nm (that's 75,000x smaller than the diameter of a strand of hair) by simply growing a film in a selected area. With traditional methods of fabrication, this would require coating a substrate with resist, patterning the resist through an exposure step, developing the image, depositing an inorganic film and then stripping the resist to give you a patterned inorganic material. We found a way of depositing this inorganic film much more simply, using a self-aligned process, where we immerse a prepatterned substrate in a solution containing a special material and then add that coated substrate to a deposition chamber and you're done. We are literally able to grow a component of a device in a controllable manner at the nanoscale.

This simple process of self-alignment is one tool required to continue scaling as it promises to simplify complex processes, saving money and reducing errors in final devices. In addition, our ability to compute [complex problems](#) is rapidly advancing, fueled by emerging technologies like AI and neuromorphic computing, each of which have very different [hardware](#) requirements in comparison to traditional semiconductor processes. Our self-alignment process provides an additional tool to fabricate non-traditional hardware that may require three dimensional structures such as cross-point arrays.

The idea of a selective deposition is not new. What is new is the synthesis and demonstration of a new material that enabled us to do this at a scale relevant for the semiconductor industry. We've primarily drawn from a depth of knowledge in the synthesis of new [materials](#) and the ability to tailor a chemical structure for demanding applications;1 in my time at Almaden, we've demonstrated this in the development of unique polymerizations,2 materials3,4 and characterization methods5,6. Once we develop methods of scaling this process, we can begin to integrate it as we build next generation hardware, whether it is for new AI hardware or making devices at the 7nm technology node or beyond. The thought of being a part of a technology advancement that could be in every smart phone or AI hardware in the future is an incredibly exciting endeavor.

**More information:** Rudy Wojtecki et al. Fifteen Nanometer Resolved Patterns in Selective Area Atomic Layer Deposition—Defectivity Reduction by Monolayer Design, *ACS Applied Materials & Interfaces* (2018). [DOI: 10.1021/acsami.8b13896](https://doi.org/10.1021/acsami.8b13896)

Provided by IBM

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