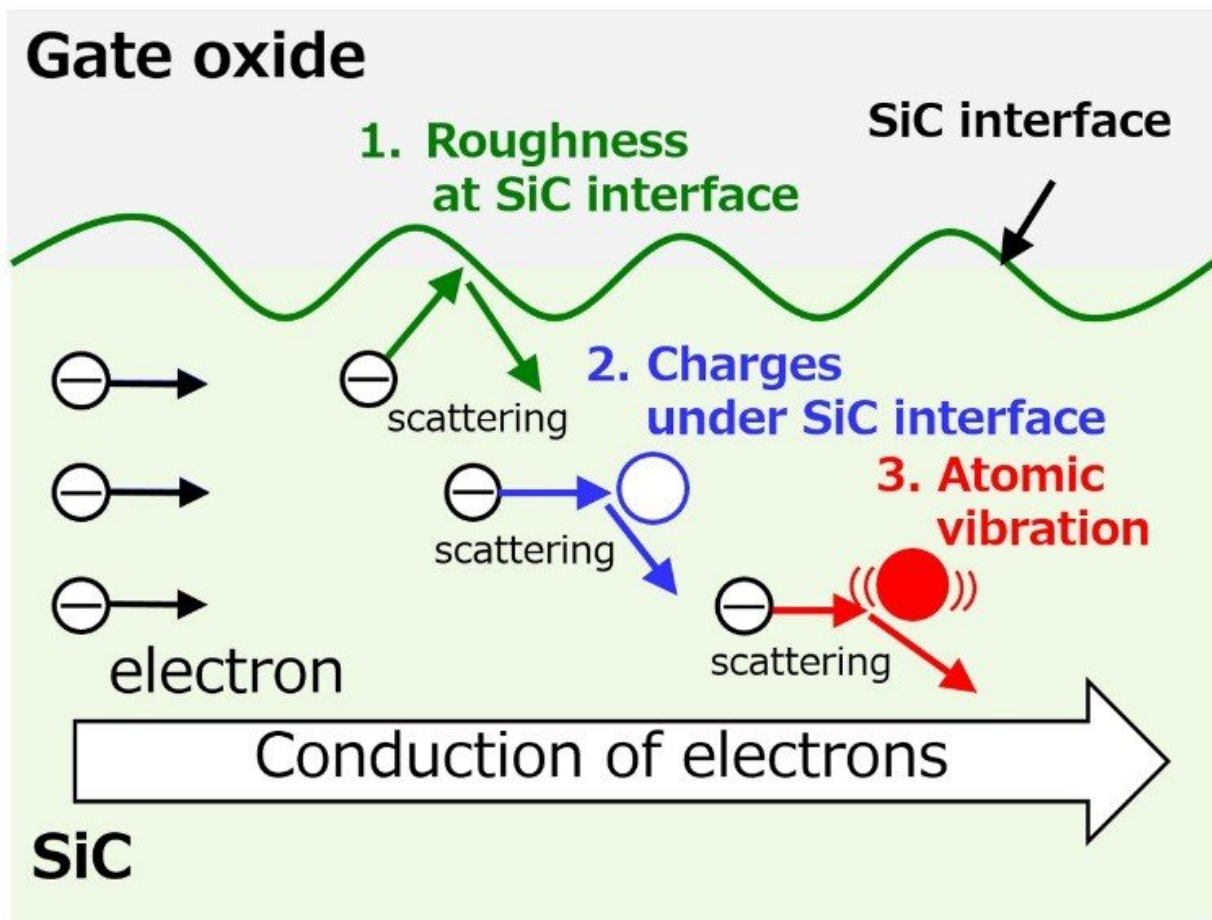


# Researchers quantify factors for reducing power semiconductor resistance by two-thirds

December 5 2017



Electron scattering under the silicon carbide (SiC) interface is limited by three factors: roughness of the SiC interface, charges under the SiC interface and atomic vibration. Credit: 2017 Mitsubishi Electric Corporation.

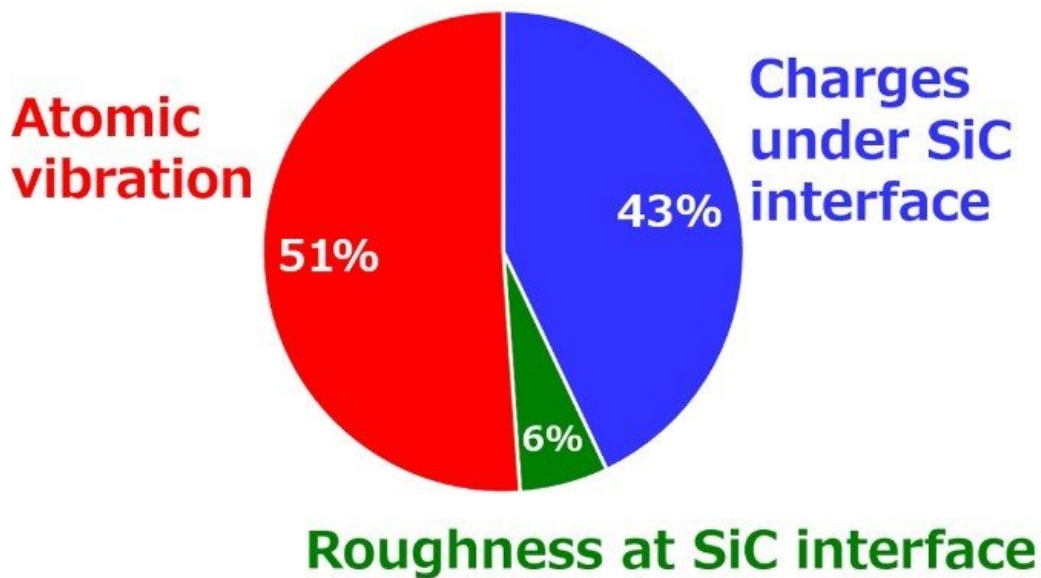
A research group in Japan announced that it has quantified for the first time the impacts of three electron-scattering mechanisms for determining the resistance of silicon carbide (SiC) power semiconductor devices in power semiconductor modules. The university-industry team has found that resistance under the SiC interface can be reduced by two-thirds by suppressing electron scattering by the charges, a discovery that is expected to reduce energy consumption in electric power equipment by lowering the resistance of SiC power semiconductors.

Electric power equipment used in home electronics, industrial machinery, trains and other apparatuses requires a combination of maximized efficiency and minimized size. Mitsubishi Electric is accelerating use of SiC devices for power semiconductor modules, which are key components in electric power equipment. SiC power devices offer lower resistance than conventional silicon power devices, so to further lower their resistance it is important to understand correctly the characteristics of the resistance under the SiC [interface](#).

"Until now, however, it had been difficult to measure separately resistance-limiting factors that determine electron scattering," says Satoshi Yamakawa, senior manager of the SiC Device Development Center at Mitsubishi Electric's Advanced Technology R&D Center.

Electron scattering focusing on atomic vibration was measured using technology from the University of Tokyo. The impact that charges and atomic vibration have on electron scattering under the SiC interface was revealed to be dominant in Mitsubishi Electric's analyses of fabricated devices. Although it has been recognized that electron scattering under the SiC interface is limited by three factors: the roughness of the SiC interface, the charges under the SiC interface and the atomic vibration, the contribution of each factor had been unclear. To confirm the impact of the charges, the researchers fabricated a planar-type SiC metal-oxide-semiconductor field-effect transistor (SiC-MOSFET), in which electrons

conduct away from the SiC interface to around several nanometers.



The research results show that the roughness of the SiC interface has little effect in limiting resistance, while charges under the SiC interface and atomic vibration are dominant factors. Credit: 2017 Mitsubishi Electric Corporation.

"We were able to confirm at an unprecedented level that the roughness of the SiC interface has little effect while charges under the SiC interface and atomic vibration are dominant factors," says Koji Kita, an associate professor at the University of Tokyo's Graduate School of Engineering and one of scientists leading the research.

Using an earlier planar-type SiC-MOSFET device for comparison,

resistance was reduced by two-thirds owing to suppression of electron scattering, which was achieved by making the electrons conduct away from the charges under the SiC interface. The previous planar-type [device](#) has the same interface structure as that of the SiC-MOSFET fabricated by the electronics maker.

For the test, Mitsubishi Electric handled the design, fabrication and analysis of the resistance-limiting factors and the University of Tokyo handled the measurement of electron-scattering factors.

"Going forward, we will continue refining the design and specifications of our SiC MOSFET to further lower the [resistance](#) of SiC [power](#) devices," says Mitsubishi Electric's Yamakawa.

Provided by University of Tokyo

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