Researchers determine optimal geometry for CBRAM computer storage

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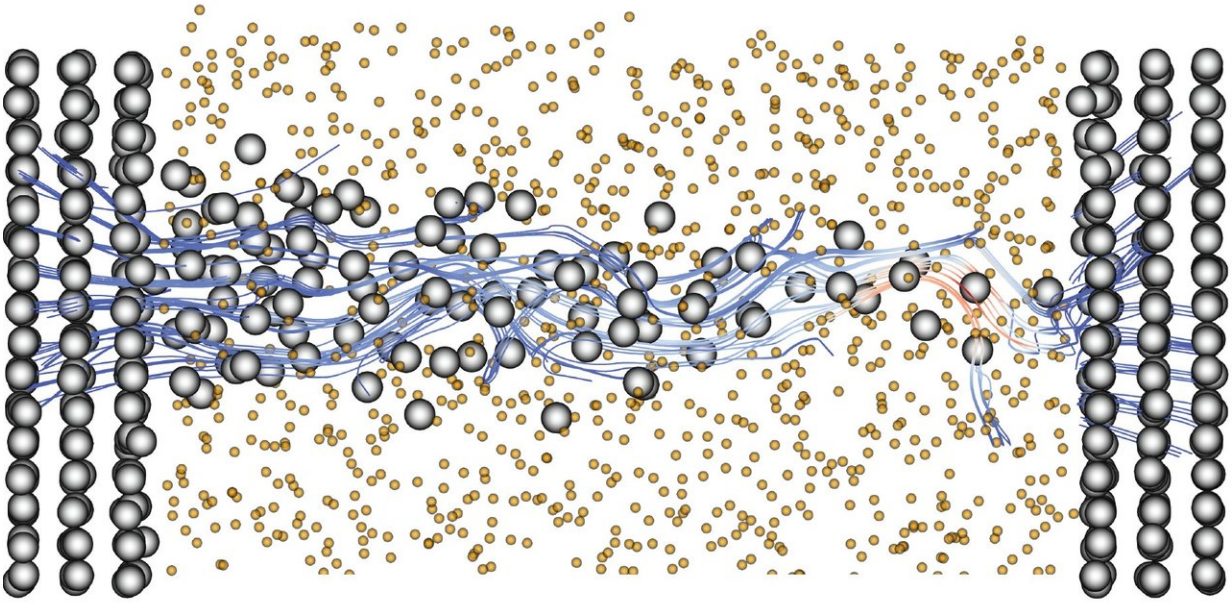

Atomic-scale computer simulation of a CBRAM cell subjected to 1mV voltage: electron trajectories (blue and red lines); copper atoms (grey); silicon and oxygen atoms (orange). Credit: Mathieu Luisier / ETH Zurich

CBRAM (conductive bridging random access memory) could play a fundamental role in memory in the future by storing data in a non-volatile (i.e., near-permanent) way. To reduce the size and power consumption of such components, it is essential to precisely understand their behaviour at the atomic level.

Mathieu Luisier, associate professor at ETH Zurich, and his team studied this type of memory, which consists of two metal electrodes separated by an insulator. The researchers developed a computer model of a CBRAM that consists of some 4500 atoms and obeys the laws of quantum mechanics governing the microscopic world. This atomic-scale simulation makes it possible to precisely describe the intensity of the current generated by a metallic nanofilament as it forms and dissolves between the electrodes.

Ten atoms thick

"This is a huge step forward," says Mathieu Luisier, who was an SNSF professor at ETH Zurich from 2011 to 2016. "Up to now, existing models could handle only about a hundred atoms." The new model accurately reproduces the electric current as well as the energy dissipated by the cell, in turn enabling calculation of its temperature. The researchers are able to observe the effect of changes in the thickness of the insulator and the diameter of the metallic filament. The findings, which were presented at the IEDM conference in San Francisco in December 2017, show that local power consumption and heat are reduced if the two electrodes are moved closer together. But only up to a certain point: electrodes that are too close are subject to the quantum tunneling effect, and the current between them is no longer controllable.

The research shows that in an optimal CBRAM geometry, the insulator is 1.5 to 2 nanometers (about 10 atoms) thick. Fabrication is still a challenge, however: machines capable of achieving such dimensions use a thermal probe lithography technique that is currently ill suited to mass production. "Today, a typical CMOS-type transistor channel measures about 20 nanometres, or ten times thicker than the CBRAM insulators we investigated," says Luisier. Consequently, Moore's law – which predicts that the size of electronic components will halve every 18–24 months – could run up against a wall within a decade.

To achieve their 4500-atom model, the researchers benefited from access to the world's third-most-powerful computer – Piz Daint – which is located at the Swiss National Supercomputing Centre (CSCS) in Lugano and can perform up to 20 million billion operations per second. This type of study requires 230 state-of-the-art graphics cards; Piz Daint has more than 4000 of them. Each card has its own CPU. "Even with this computational power, it takes ten hours or so to simulate one memory and to determine its electrical characteristics," says Luisier.

More information: F. Ducry et al.: Ab-initio Modeling of CBRAM Cells: from Ballistic Transport Properties to Electro-Thermal Effects. Proceedings of the IEDM Conference 2017. (pdf)

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