Managing stress helps transistor performance

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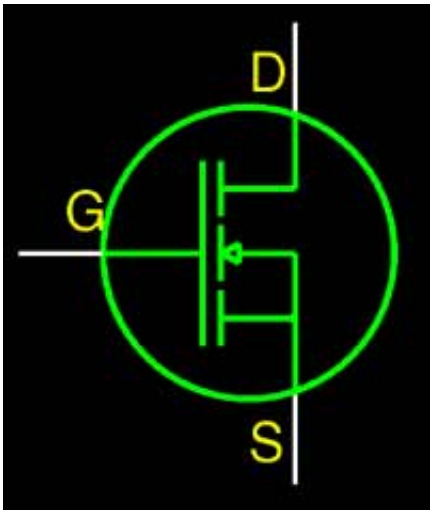

Tensile mechanical stress can have a useful effect for some transistors, where the resulting atomic strain allows its current-carrying electron-hole pairs better mobility. However, when that stress is applied to the whole device, as is a popular approach via use of what's called contact etching stop layers (CESLs), the drift region adjacent to the stretched channel is compressed and results in reduced performance.

A research team in China have developed a new CESL method that introduces tensile stress into both the channel and the drift region, improving overall performance by offering low drift resistance, high cut-

off frequency and desirable breakdown characteristics. Their work is described in an article appearing this week in the journal *AIP Advances*.

The team of researchers became interested in the method because of work done on strained silicon techniques. During research on strained meta-oxide semiconductor field effect transistors (MOSFETs), researchers saw that the stress in the source/drain region was inverse to the channel region stress. Based on these observations, they began to study how they might use this phenomenon in a way that could enhance performance.

This new research focused on partial silicon-on-insulator (PSOI) devices that introduce tensile stress into both the channel and the drift region using the CESLs. Simulation results also showed that the PSOI device offers better frequency performance and driving capability than unstrained devices.

"The most difficult thing for us was to find a low cost, CMOS-compatible method for applying mechanical stress," said Xiangzhan Wang, from the University of Electronic Science and Technology of China. "During the manufacturing process, the wafer bends as the stress film (Si3N4) grows, which creates a problem in holding the wafer in process equipment."

The experiment results, however, increased confidence that the new strain technique could not only be applied to small devices, but also to rather large devices to yield performance improvement. With the results, even the research team was surprised at the level of improvement it provided to their simulations.

"In our simulation, the fully tensile strained PSOI n-type LDMOSFET showed a 20-30 percent driving current improvement over normal Si LDMOSFET," Wang said. "But when we used this strain method with a

commercial Si LDMOS product, the driving current doubled yielding a current increase of more than 100 percent, which was quite surprising for us."

While this work has contributed to understanding of the strained Si mechanisms, there is still more to improve and understand.

"The next research directions for the team are to optimize the fabrication process for these devices in order to obtain better stability and to try applying the same method to a nonsymmetrical device such as a tunnel FET," Wang said.

More information: "Fully tensile strained partial silicon-on-insulator n-type lateral-double-diffused metal-oxide-semiconductor field effect transistor using localized contact etching stop layers," Xiangzhan Wang, Changgui Tan, Xi Zou, Yi Zhang, Jianhua Pan, and Yang Liu. *AIP Advances*, May 16, 2017 DOI: 10.1063/1.4983214