Self-assembly technique could lead to long-awaited, simple method for making smaller microchip patterns

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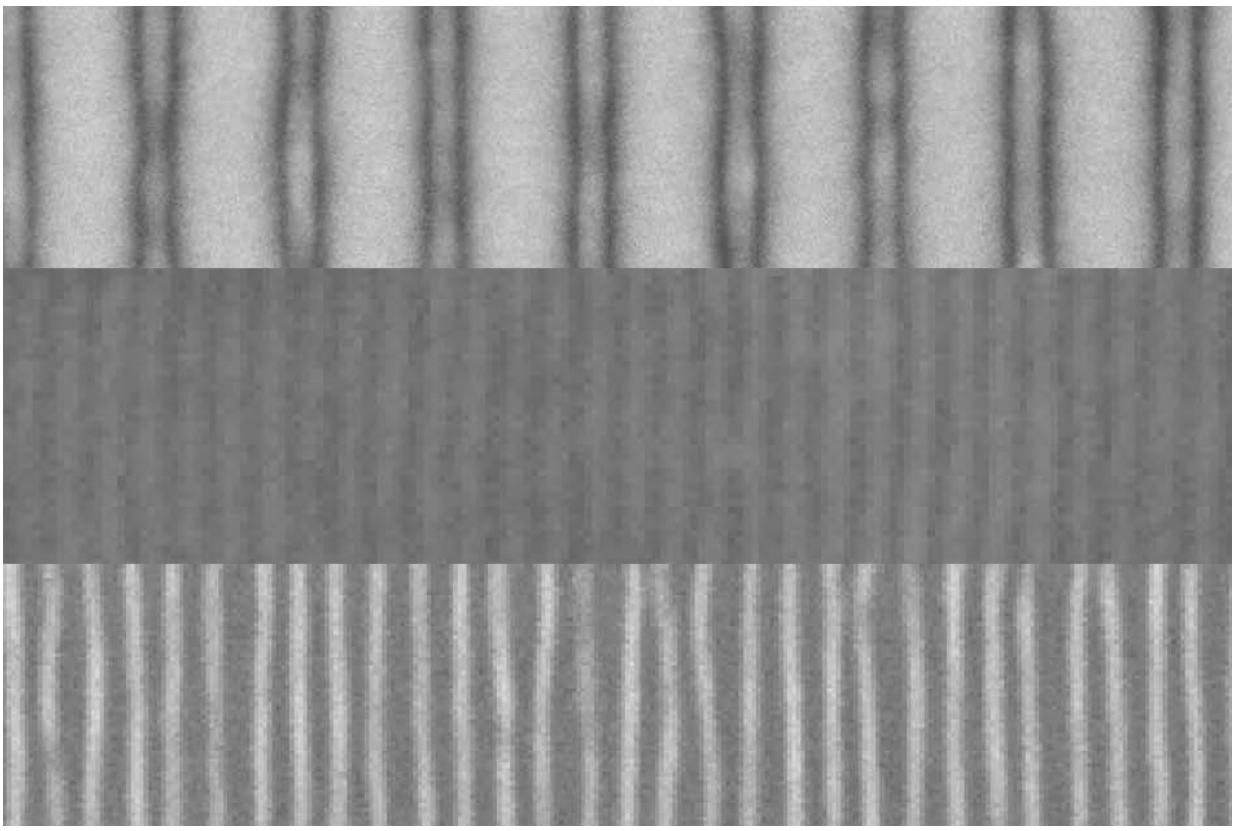

These scanning electron microscope images show the sequence of fabrication of fine lines by the team's new method. First, an array of lines is produced by a conventional electron beam process (top). The addition of a block copolymer material and a topcoat result in a quadrupling of the number of lines (center). Then the topcoat is etched away, leaving the new pattern of fine lines exposed (bottom). Credit: Massachusetts Institute of Technology

For the last few decades, microchip manufacturers have been on a quest to find ways to make the patterns of wires and components in their microchips ever smaller, in order to fit more of them onto a single chip and thus continue the relentless progress toward faster and more powerful computers. That progress has become more difficult recently, as manufacturing processes bump up against fundamental limits involving, for example, the wavelengths of the light used to create the patterns.

Now, a team of researchers at MIT and in Chicago has found an approach that could break through some of those limits and make it possible to produce some of the narrowest wires yet, using a process that could easily be scaled up for mass manufacturing with standard kinds of equipment.

The new findings are reported this week in the journal *Nature Nanotechnology*, in a paper by postdoc Do Han Kim, graduate student Priya Moni, and Professor Karen Gleason, all at MIT, and by postdoc Hyo Seon Suh, Professor Paul Nealey, and three others at the University of Chicago and Argonne National Laboratory. While there are other methods that can achieve such fine lines, the team says, none of them are cost-effective for large-scale manufacturing.

The new approach uses a self-assembly technique in which materials known as block copolymers are covered by a second polymer. They are deposited on a surface by first heating the precursor so it vaporizes, then allowing it to condense on a cooler surface, much as water condenses on the outside of a cold drinking glass on a hot day.

"People always want smaller and smaller patterns, but achieving that has been getting more and more expensive," says Gleason, who is MIT's

associate provost as well as the Alexander and I. Michael Kasser (1960) Professor of Chemical Engineering. Today's methods for producing features smaller than about 22 nanometers (billionths of a meter) across generally require building up an image line by line, by scanning a beam of electrons or ions across the chip surface—a very slow process and therefore expensive to implement at large scale.

The new process uses a novel integration of two existing methods. First, a pattern of lines is produced on the chip surface using standard lithographic techniques, in which light shines through a negative mask placed on the chip surface. That surface is chemically etched so that the areas that were illuminated get dissolved away, leaving the spaces between them as conductive "wires" that connect parts of the circuit.

Then, a layer of material known as a block copolymer—a mix of two different polymer materials that naturally segregate themselves into alternating layers or other predictable patterns—is formed by spin coating a solution. The block copolymers are made up of chain-like molecules, each consisting of two different polymer materials connected end-to-end.

"One half is friendly with oil, the other half is friendly with water," Kim explains. "But because they are completely bonded, they're kind of stuck with each other." The dimensions of the two chains predetermine the sizes of layers or other patterns they will assemble themselves into when they are deposited.

Finally, a top, protective polymer layer is deposited on top of the others using chemical vapor deposition (CVD). This top coat, it turns out, is a key to the process: It constrains the way the block copolymers self-assemble, forcing them to form into vertical layers rather than horizontal ones, like a layer cake on its side.

The underlying lithographed pattern guides the positioning of these layers, but the natural tendencies of the copolymers cause their width to be much smaller than that of the base lines. The result is that there are now four (or more, depending on the chemistry) lines, each of them a fourth as wide, in place of each original one. The lithographed layer "controls both the orientation and the alignment" of the resulting finer lines, explains Moni.

Because the top polymer layer can additionally be patterned, the system can be used to build up any kind of complex patterning, as needed for the interconnections of a microchip.

Most microchip manufacturing facilities use the existing lithographic method, and the CVD process itself is a well-understood additional step that could be added relatively easily. Thus, implementing the new method could be much more straightforward than other proposed methods of making finer lines, such as the use of extreme ultraviolet light, which would require the development of new light sources and new lenses to focus the light. With the new method, Gleason says, "you wouldn't need to change all those machines. And everything that's involved are well-known materials."

More information: Hyo Seon Suh et al, Sub-10-nm patterning via directed self-assembly of block copolymer films with a vapour-phase deposited topcoat, *Nature Nanotechnology* (2017). DOI: 10.1038/NNANO.2017.34

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