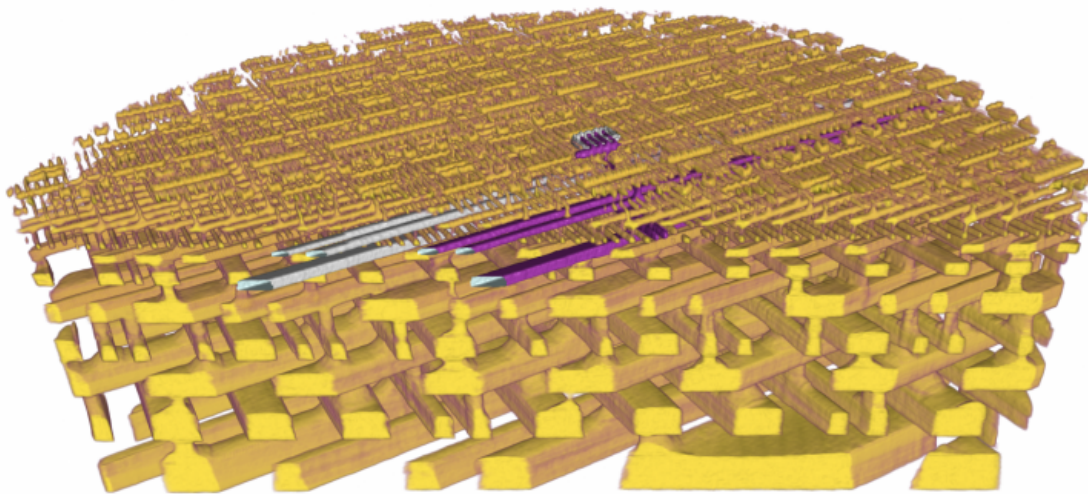


3-D X-ray imaging makes the finest details of a computer chip visible

March 16 2017, by Paul Piwnicki



3-D representation of the internal structure of a microchip (an Intel processor). The view shown is exactly at the level where the transistors are. The material in yellow is copper — showing the processor's circuit connections which link the individual transistors with each other. To illustrate, several interconnections whose lines could be followed through the volume examined have been coloured. The lines shown individually are around 45 nanometres wide (45 millionths of a millimetre); in all, a piece of the processor of around 10 micrometres (10

thousandths of a millimetre) in diameter was examined. Credit: Paul Scherrer Institute/Mirko Holler

Researchers of the Paul Scherrer Institute PSI have made detailed 3-D images of a commercially available computer chip. This marks the first time a non-destructive method has visualized the paths of a chip's internal wiring (just 45 nanometres—45 millionths of a millimetre—wide) and its 34-nanometre-high transistors clearly without distortions or deformations. It is a major challenge for manufacturers to determine if, in the end, the structure of their chips conforms to the specifications. Thus these results represent one important application of an X-ray tomography method that the PSI researchers have been developing for several years. In their experiment, the researchers examined a small piece that they had cut out of the chip beforehand. This sample remained undamaged throughout the measurement. The goal now is to extend the method in such a way that it can be used to examine complete chips. The researchers conducted the experiments at the Swiss Light Source SLS of the Paul Scherrer Institute.

They report their results in the latest edition of the journal *Nature*.

The electrical wiring in many of the electronic chips in our computers and mobile phones are just 45 nanometres wide, the transistors 34 nanometres high. While it is standard practice today to produce structures this delicate, it remains a challenge to measure the exact structure of a finished chip in detail in order to check, for example, if it is built according to the specifications. Nowadays, for such examinations, manufacturers mainly use a method in which layer after layer of the chip is removed and then, after each step, the surface is examined with an electron microscope; this is known as FIB/SEM—focused ion beam/scanning electron microscope imaging.

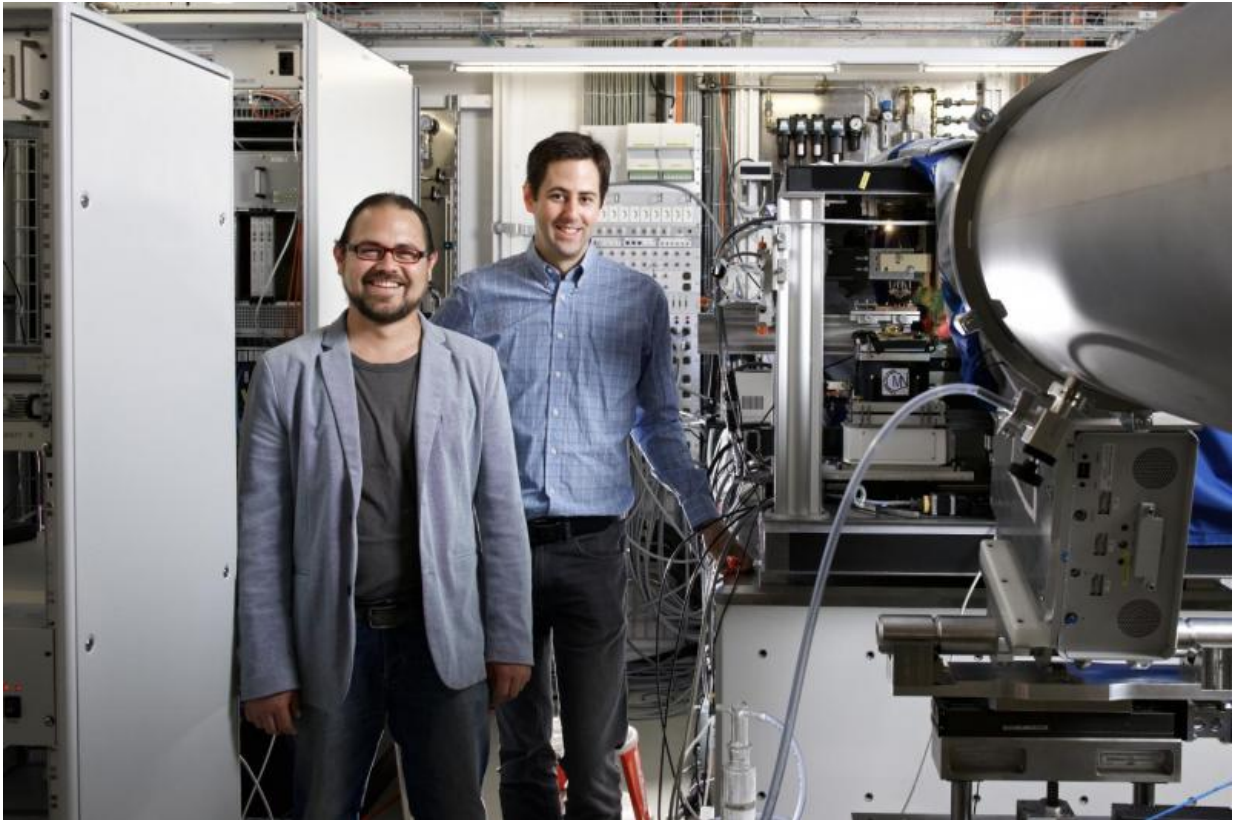
Now researchers of the Paul Scherrer Institute PSI have used X-rays to achieve non-destructive 3-D imaging of a chip, so that the paths of the conducting lines and the positions of the individual transistors and other circuit elements became clearly visible. The image resolution we were able to produce is comparable to the conventional FIB/SEM examination method, explains Mirko Holler, leader of the project. But we were able to avoid two significant disadvantages: Firstly, the sample remained undamaged, and we have complete information about the [three-dimensional structure](#). Secondly, we avoided distortions of the images that arise in FIB/SEM if the surface of the individual slice is not exactly planar.

Positioned with nanometre precision

For their study, the researchers used a special tomographic method (ptychotomography) that they have developed and enhanced over the course of recent years, and which today offers the worldwide best resolution of 15 nanometres (15 millionths of a millimetre) for examination of a comparably large volume. In the experiment the object to be studied is X-rayed at precisely determined places with light from the Swiss Light Source SLS of the Paul Scherrer Institute—for each illuminated spot a detector then measures the X-ray light pattern after its passage through the sample. The sample is then rotated in small steps and then X-rayed again step-wise after each turn. From the whole set of data obtained, the three-dimensional structure of the sample can be determined. With these measurements, the position of the sample must be known to a precision of just a few nanometres—that was one of the particular challenges in setting up our experimental station, Holler says.

In their experiment the researchers examined small pieces of two chips—a detector chip developed at PSI and a commercially available computer chip. Each piece was about 10 micrometres (that is, 10 thousandths of a millimetre) in size. While the examination of an entire

chip with the present measurement setup is not possible, the method's advantages are brought to bear even in this form, so that the first prospective users have already expressed an interest in conducting measurements at PSI.

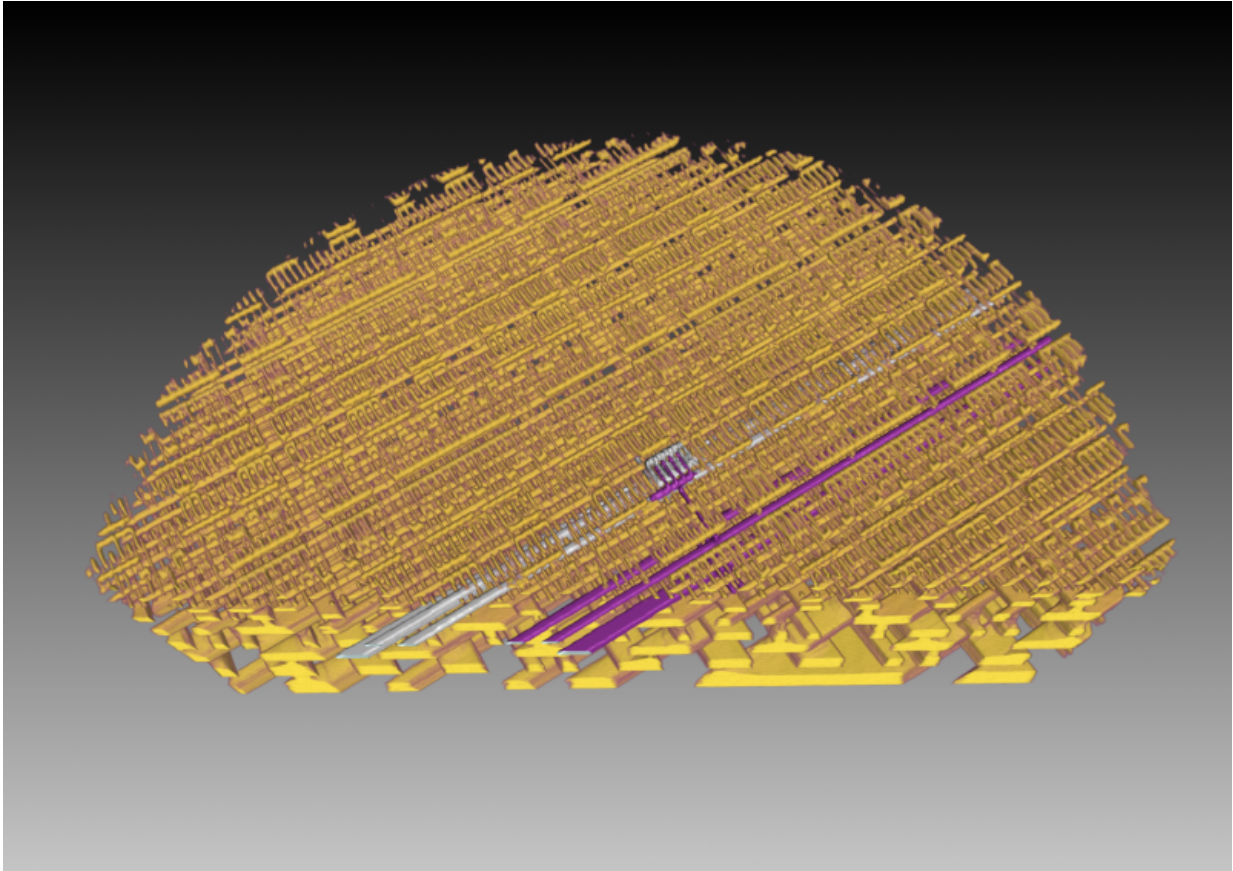


PSI researchers Mirko Holler (right) and Manuel Guizar-Sicairos at the cSAXS beamline of the Swiss Light Source SLS of the Paul Scherrer Institute. Here they made the three-dimensional structure of a microchip visible. Credit: Paul Scherrer Institute/Markus Fischer

The goal: to examine entire microchips

We are currently starting to extend the method in such a way that it can

be used to examine entire microchips within an acceptable measurement time. Then it will also be possible to study the same area of a [chip](#) multiple times, for example to observe how it changes under external influences, explains Gabriel Aeppli, head of the Synchrotron Radiation and Nanotechnology Division at the PSI.



A second 3-D representation of the internal structure of a microchip (an Intel processor). Credit: Paul Scherrer Institute/Mirko Holler

More information: Mirko Holler et al. High-resolution non-destructive three-dimensional imaging of integrated circuits, *Nature*

(2017). [DOI: 10.1038/nature21698](https://doi.org/10.1038/nature21698)

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