New circuit scheme would greatly increase the accuracy of high-density spin-based data storage

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While we aspire to store increasing amounts of digital data on ever smaller devices, conventional memory technologies based on electron charge are reaching a physical limit on how much they can store in a given space. Alternative storage methods are urgently needed.

Kien Trinh, Sergio Ruocco and Massimo Alioto at the A*STAR Data Storage Institute and National University of Singapore are investigating a promising storage technique called spin-transfer torque magnetic random-access memory (STT-MRAM). In their pursuit, the researchers have developed a voltage-boosting scheme for an STT-MRAM system, which greatly reduces errors incurred when reading data.

STT-MRAM works by exploiting electrons' intrinsic angular momentum, or spin, rather than their charge. Electron spin can take only two values—up or down—and a standard electrical current contains approximately equal numbers of each. STT-MRAM uses a spin-polarized current, which has more of one spin type than the other, to exert a torque on magnetized 'bitcells'. This flips the bitcell orientation to high or low states and thereby writes binary data. To read data, the surrounding circuitry must then detect small changes in the resistance of the bitcell, a difficult task to achieve without errors.

"In the physical process of reading STT-MRAM there is an established trade-off between read disturbance (the chance of unintentionally

flipping the bitcell when you read it) and read decision (reading the wrong value currently stored in the bitcell)," says Trinh. "To lower the read disturbance, the read current has to be small. However, a larger read current helps us distinguish between the high and low resistance states of the bitcell." In other words, if you reduce one error, you increase the other.

Trinh and co-workers trialed a new read scheme in which the voltage in the system was boosted by switched capacitors. They performed extensive statistical simulations to find optimum electronic design settings that minimize the impact of natural variations.

"We achieved a rate of just one error per billion bitcell reads, compared to the conventional sensing scheme which has one per ten million," says Alioto. "What's more, our system is one of the first that can achieve so few errors while remaining suitable for low-power and low-voltage applications."

The team are hopeful they can prove their design concepts on real devices in the near future, and contribute to the commercialization of this emerging technology. "We think STT-MRAM could be available on the consumer market within three to five years," says Ruocco.

More information: Quang Kien Trinh et al. Novel Boosted-Voltage Sensing Scheme for Variation-Resilient STT-MRAM Read, *IEEE Transactions on Circuits and Systems I: Regular Papers* (2016). DOI: 10.1109/TCSI.2016.2582203

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