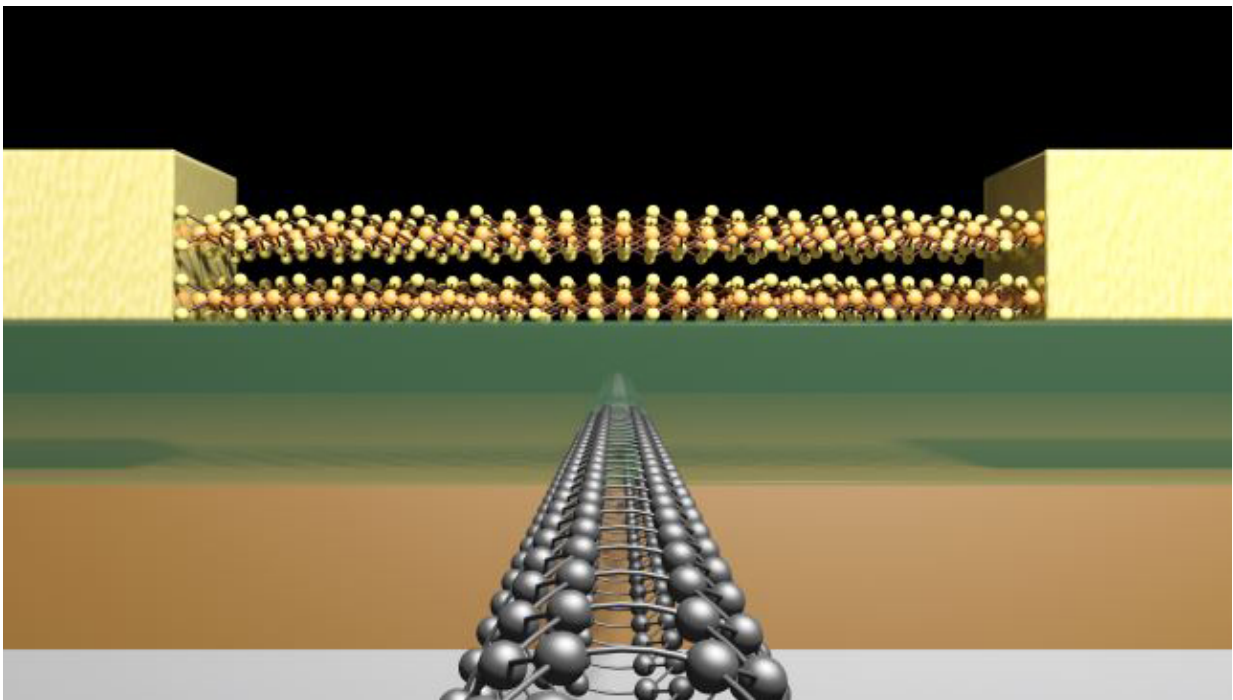


Researchers use novel materials to build smallest transistor with 1-nanometer carbon nanotube gate

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MoS₂ transistor with 1-nanometer carbon nanotube gate. Credit: Sujay Desaj

For more than a decade, engineers have been eyeing the finish line in the race to shrink the size of components in integrated circuits. They knew that the laws of physics had set a 5-nanometer threshold on the size of transistor gates among conventional semiconductors, about one-quarter

the size of high-end 20-nanometer-gate transistors now on the market.

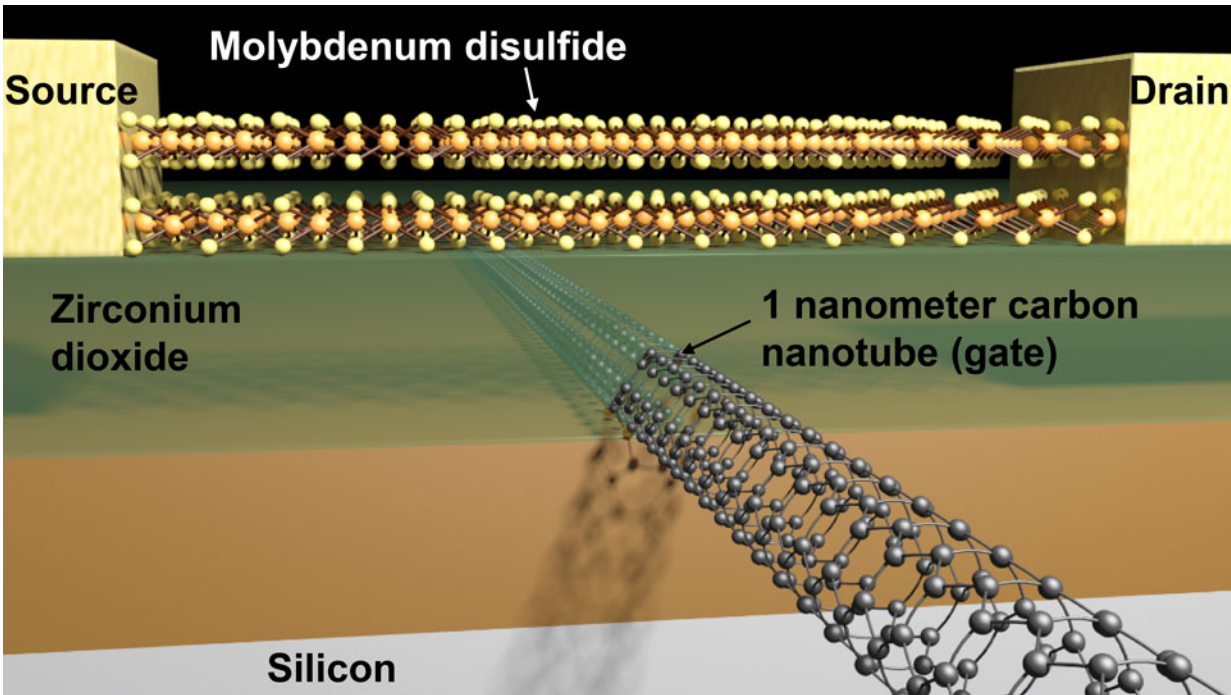
Some laws are made to be broken, or at least challenged.

A research team led by faculty scientist Ali Javey at the Department of Energy's Lawrence Berkeley National Laboratory (Berkeley Lab) has done just that by creating a transistor with a working 1-nanometer gate. For comparison, a strand of human hair is about 50,000 nanometers thick.

"We made the smallest transistor reported to date," said Javey, a lead principal investigator of the Electronic Materials program in Berkeley Lab's Materials Science Division. "The gate length is considered a defining dimension of the transistor. We demonstrated a 1-nanometer-gate transistor, showing that with the choice of proper materials, there is a lot more room to shrink our electronics."

The key was to use carbon nanotubes and molybdenum disulfide (MoS_2), an engine lubricant commonly sold in auto parts shops. MoS_2 is part of a family of materials with immense potential for applications in LEDs, lasers, nanoscale transistors, solar cells, and more.

The findings will appear in the Oct. 7 issue of the journal *Science*. Other investigators on this paper include Jeff Bokor, a faculty senior scientist at Berkeley Lab and a professor at UC Berkeley; Chenming Hu, a professor at UC Berkeley; Moon Kim, a professor at the University of Texas at Dallas; and H.S. Philip Wong, a professor at Stanford University.



A schematic of a transistor with a molybdenum disulfide channel and 1-nanometer carbon nanotube gate. Credit: Sujay Desai/Berkeley Lab

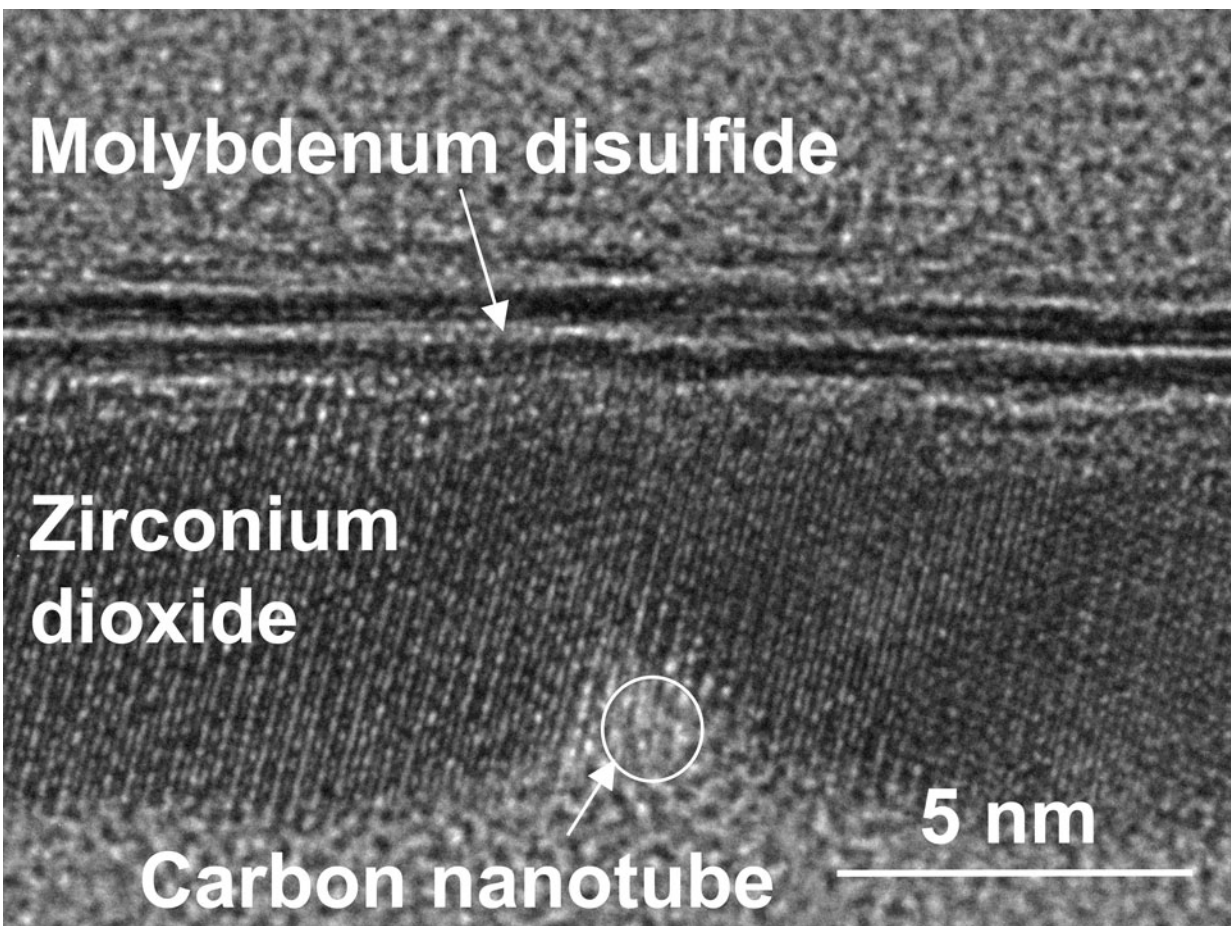
The development could be key to keeping alive Intel co-founder Gordon Moore's prediction that the density of transistors on [integrated circuits](#) would double every two years, enabling the increased performance of our laptops, mobile phones, televisions, and other electronics.

"The semiconductor industry has long assumed that any gate below 5 nanometers wouldn't work, so anything below that was not even considered," said study lead author Sujay Desai, a graduate student in Javey's lab. "This research shows that sub-5-nanometer [gates](#) should not be discounted. Industry has been squeezing every last bit of capability out of silicon. By changing the material from silicon to MoS₂, we can make a transistor with a gate that is just 1 nanometer in length, and operate it like a switch."

When 'electrons are out of control'

Transistors consist of three terminals: a source, a drain, and a gate. Current flows from the source to the drain, and that flow is controlled by the gate, which switches on and off in response to the voltage applied.

Both silicon and MoS₂ have a crystalline lattice structure, but electrons flowing through silicon are lighter and encounter less resistance compared with MoS₂. That is a boon when the gate is 5 nanometers or longer. But below that length, a quantum mechanical phenomenon called tunneling kicks in, and the gate barrier is no longer able to keep the electrons from barging through from the source to the drain terminals.



Transmission electron microscope image of a cross section of the transistor. It shows the ~ 1 nanometer carbon nanotube gate and the molybdenum disulfide semiconductor separated by zirconium dioxide which is an insulator. Credit: Qingxiao Wang, UT Dallas

"This means we can't turn off the transistors," said Desai. "The electrons are out of control."

Because electrons flowing through MoS₂ are heavier, their flow can be controlled with smaller gate lengths. MoS₂ can also be scaled down to atomically thin sheets, about 0.65 nanometers thick, with a lower dielectric constant, a measure reflecting the ability of a material to store energy in an electric field. Both of these properties, in addition to the mass of the electron, help improve the control of the flow of current inside the transistor when the gate length is reduced to 1 nanometer.

Once they settled on MoS₂ as the semiconductor material, it was time to construct the gate. Making a 1-nanometer structure, it turns out, is no small feat. Conventional lithography techniques don't work well at that scale, so the researchers turned to carbon nanotubes, hollow cylindrical tubes with diameters as small as 1 nanometer.

They then measured the electrical properties of the devices to show that the MoS₂ transistor with the carbon nanotube gate effectively controlled the flow of electrons.

"This work demonstrated the shortest transistor ever," said Javey, who is also a UC Berkeley professor of electrical engineering and computer sciences. "However, it's a proof of concept. We have not yet packed these transistors onto a chip, and we haven't done this billions of times

over. We also have not developed self-aligned fabrication schemes for reducing parasitic resistances in the device. But this work is important to show that we are no longer limited to a 5-nanometer gate for our transistors. Moore's Law can continue a while longer by proper engineering of the semiconductor material and device architecture."

More information: "MoS2 transistors with 1-nanometer gate lengths" *Science*, [science.sciencemag.org/cgi/doi ... 1126/science.aah4698](https://science.sciencemag.org/cgi/doi/10.1126/science.aah4698)

Provided by Lawrence Berkeley National Laboratory

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