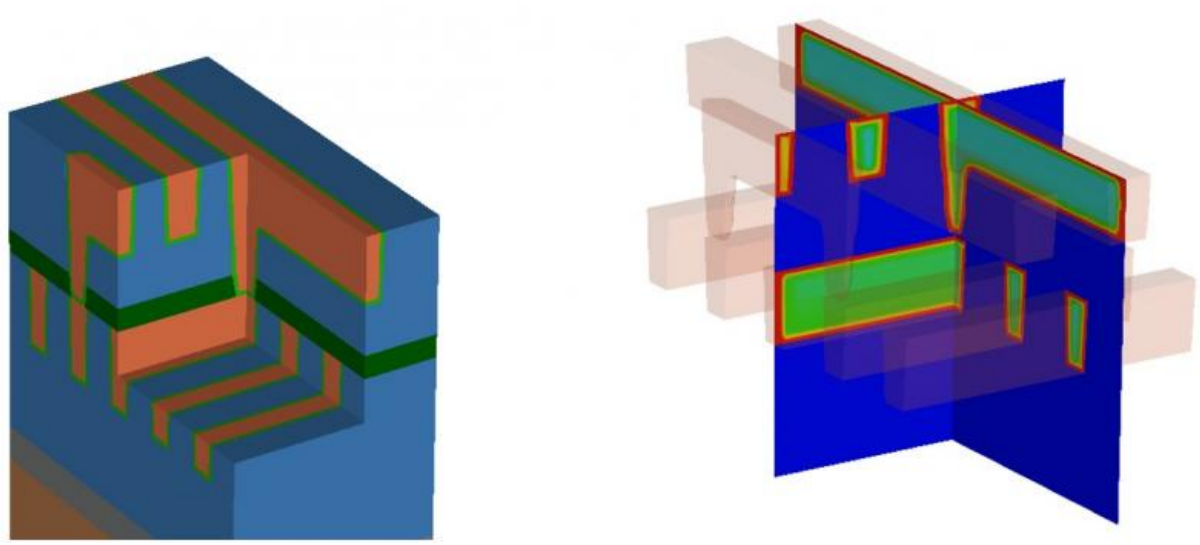
Interconnect resistivity model to enable early screening of interconnect technology options at advanced nodes

July 12 2016



Caption: 3D model of a multilayer interconnect stack (a) after process emulations using the Synopsys Sentaurus Process Explorer and 3D local resistivity profile (b) within wires and vias. Credit: IMEC

Nano-electronics research center imec and Synopsys, Inc. today announced an interconnect resistivity model to support the screening and selection of alternative interconnect metals and liner-barrier materials at the 7nm node and beyond. With the continued scaling of advanced process nodes, the impact of parasitic interconnect resistance on the

switching delay of standard cells rises considerably. The new model developed through this collaboration enables the evaluation of interconnect material and process options through simulations in the early stages of technology development, when wafer data is not available, and in the process optimization and integration stages of technology development, where it reduces expensive and time-consuming wafer-based iterations.

"We have already released to our partners a number of sets of model parameters related to various liner/barrier systems for Cu metallization or to alternative metals, such as Ru and Co, which they will use to screen metallization options for next-generation interconnect technologies," stated Dan Mocuta, director, Logic Device and Integration at imec.

To use the new resistivity model, customers simulate the fabrication of the interconnect structure in 3D using the Synopsys process emulation tool Process Explorer, and then simulate the wire and via resistance in Raphael, the Synopsys gold standard interconnect field solver. This simulation flow accounts for the impact of layout rules, multi-patterning flows, and process-induced 3D features on the resistance of any conductive net in a multilayer interconnect stack, thereby predicting the influence of material, process and patterning choices on the interconnect resistance at scaled dimensions.

Imec has calibrated the resistivity model to wafer data for Cu, W, Ru and Co interconnects.

"The new resistivity model developed through this collaboration with imec is an important component of our pre-wafer simulation solution to enable our mutual customers to perform early screening of interconnect technology options at advanced nodes," said Dr. Howard Ko, senior vice president and general manager of the Silicon Engineering Group at Synopsys.

Provided by IMEC