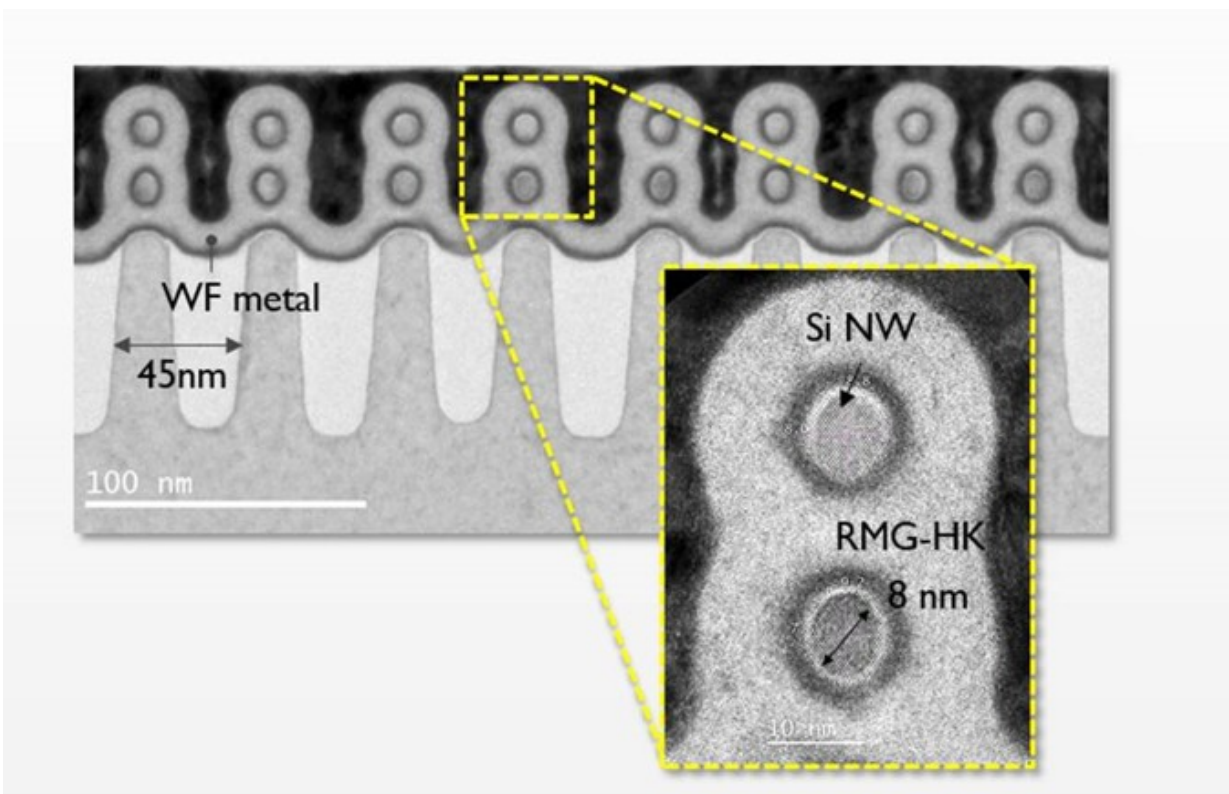


Imec demonstrates gate-all-around MOSFETs with lateral silicon nanowires at scaled dimensions

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TEM images of an NMOS GAASiNWFET(LG=70nm):(a)overview of the SiNW array; (b)detailed view of two stacked SiNWs. Credit: IMEC RSS feed

Today, at the 2016 Symposia on VLSI Technology & Circuits, nano-

electronics research center imec presented gate-all-around (GAA) n- and p-MOSFET devices made of vertically stacked horizontal silicon (Si) nanowires (NWs) with a diameter of only 8-nm. The devices, which were fabricated on bulk Si substrates using an industry-relevant replacement metal gate (RMG) process, have excellent short-channel characteristics ($SS = 65$ mV/dec, $DIBL = 42$ mV/V for $LG = 24$ nm) at performance levels comparable to finFET reference devices.

GAA devices architectures offer optimal electrostatic control, thereby enabling ultimate CMOS [device](#) scaling. In addition, horizontal NWs are a natural extension of RMG finFETs, in contrast to vertical NWs which require more disruptive technology changes. Furthermore, stacking of NWs maximizes the drive current per footprint. Imec successfully combined these three aspects, and, for the first time, demonstrated vertically stacked horizontal Si NWs at scaled dimensions: 8-nm-diameter wires, 45-nm lateral pitch, and 20-nm vertical separation.

Compared to the conventional bulk FinFET flow, imec implemented two major differences in the process flow. First, shallow trench isolation (STI) densification at 750°C resulted to preserve sharp silicon-germanium (SiGe)/Si interfaces, which is essential for well-controlled Si NW release. Second, a low-complexity ground plane doping scheme was applied, suppressing the bottom parasitic channel.

"By demonstrating stacked nanowires with solid electrostatic control, at scaled dimensions, and using an industry-relevant RMG process on bulk silicon substrates, imec has achieved breakthrough results that can pave the way to realizing sub-10nm technology nodes," stated Dan Mocuta, Director Logic Device and Integration at imec. "The upcoming research phase will focus on achieving even denser pitches and on leveraging this knowledge to develop gate-all-around lateral nanowire CMOS devices."

Imec's research into advanced logic scaling is performed in cooperation

with imec's key partners in its core CMOS programs including GlobalFoundries, Intel, Micron, SK Hynix, Samsung, TSMC, Huawei, Qualcomm and Sony.

Provided by IMEC

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