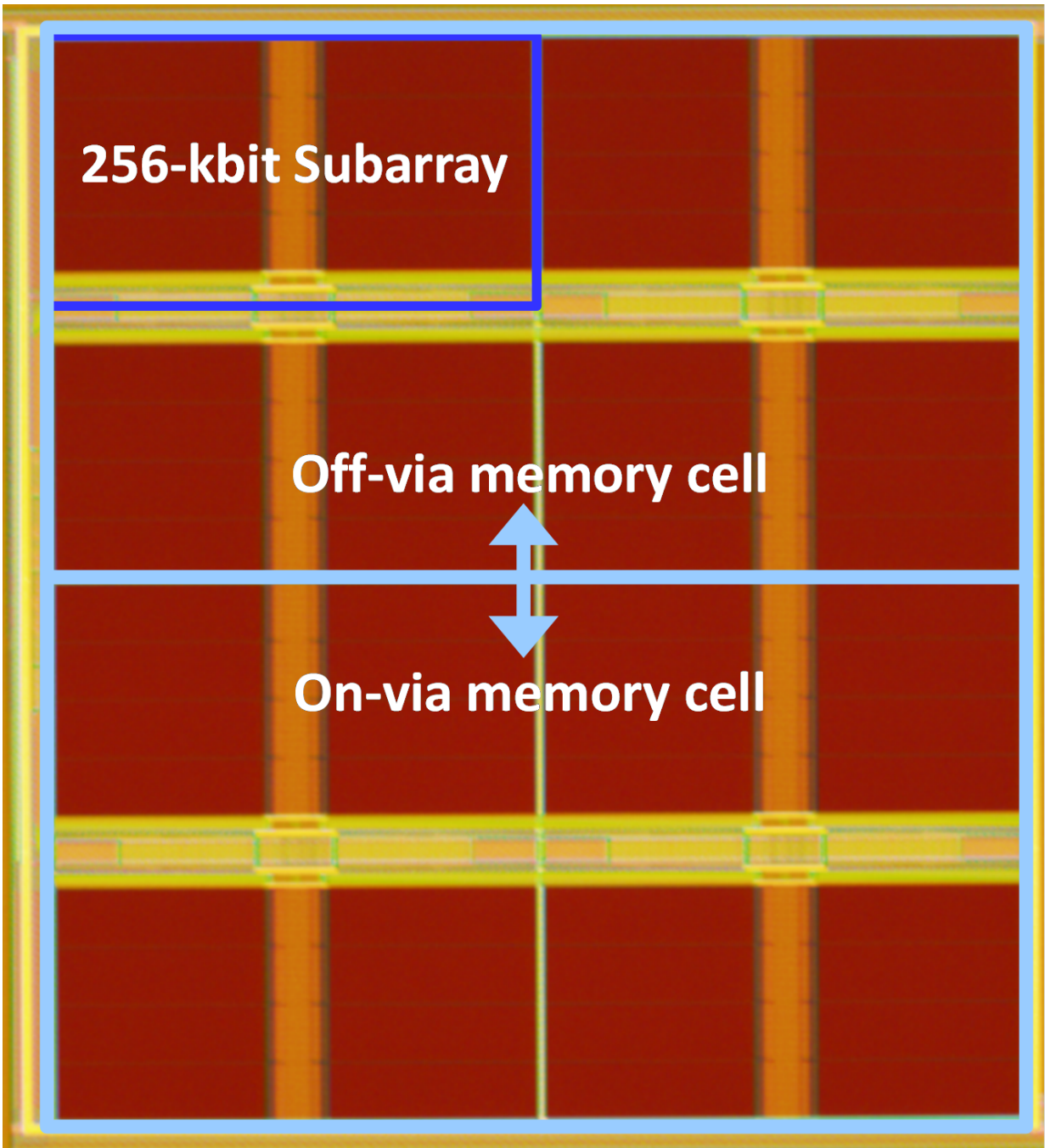


New technology reduces 30 percent chip area of STT-MRAM while increasing memory bit yield by 70 percent

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Fabricated 2-Mbit MRAM test chip for verifying the developed MTJ formation technology directly on via hole in VLSI. Credit: Yoichi Oshima

In a world first, researchers from Tohoku University have successfully

developed a technology to stack magnetic tunnel junctions (MTJ) directly on the vertical interconnect access (via) without causing deterioration to its electric/magnetic characteristics. The via in an integrated circuit design is a small opening that allows a conductive connection between the different layers of a semiconductor device.

This new discovery will be particularly significant in reducing the chip area of spin-transfer torque magnetic random access [memory](#) (STT-MRAM), making its commercialization more practical.

The team led by Professor Tetsuo Endoh, Director of the Center for Innovative Integrated Electronic Systems (CIES), focused on reducing the memory cell area of STT-MRAMs in order to lower manufacturing costs, making them competitive with conventional semiconductor memories like dynamic [random access memory](#) (DRAM).

Because MTJs use magnetic properties, the quality of the surface between the MTJ and its lower electrode is important. If the surface area is not smooth, the electric/magnetic characteristics of the MTJ will degrade. For this reason, placing an MTJ directly on the via holes in STT-MRAMs has been avoided until now, although it increases the size of the memory cell.

Endoh's group has tackled the issue by developing a special polishing process technology to prevent any interference between the MTJ and its lower electrode. The technology's effectiveness was successfully verified by an experiment using single-MTJ test chips.

To further test the success of this development, a 2-Mbit STT-MRAM test chip integrating the new technology has been designed to verify the space needed for the integrated circuits—this includes more than 1 million MTJs.

"Not only does this test chip show a 70% improvement in its memory bit yield compared to standard STT-MRAM, but its memory cell area is reduced by 30%," says Endoh. "It will be very effective for reducing the chip area of MRAM."

CIES develops material, process, circuit and [test](#) technologies in integrated electronic systems. The center's main focus is on developing high-performance, low-power technologies for a more energy-efficient society.

The results of this research were presented at the IEEE International Memory Workshop in France on May 16, 2016.

More information: Demonstration of yield improvement for on-via MTJ using a 2-Mbit 1T-1MTJ STT-MRAM test chip, *Proceedings of 2016 IEEE International Memory Workshop (2016)*

Provided by Tohoku University

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