Internet on a chip: Researchers step towards energy-efficient multicore chips

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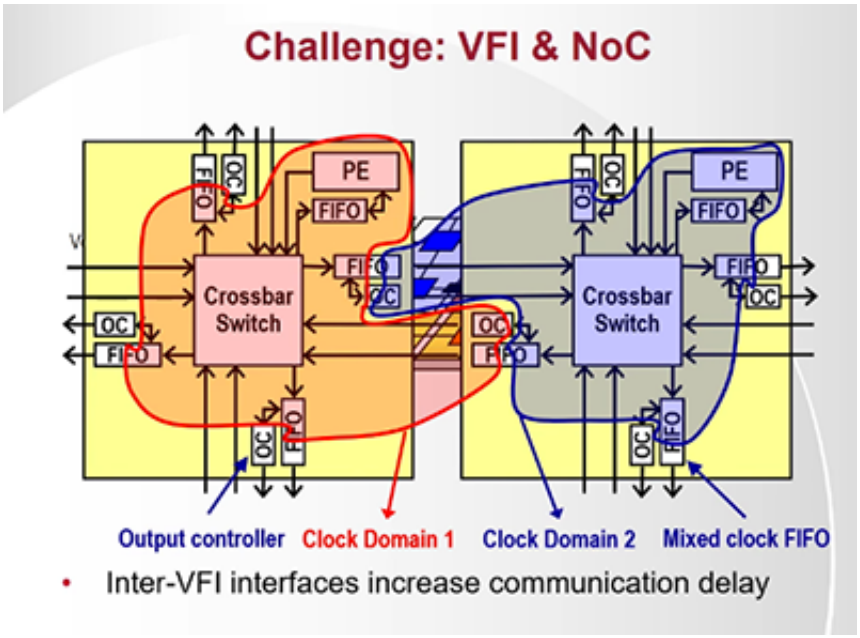


Credit: Carnegie Mellon University Electrical and Computer Engineering

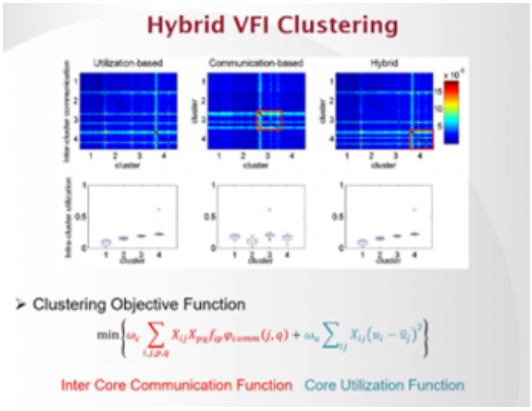
In their recent paper, Wireless NoC for VFI-enabled multicore chip design: performance evaluation and design trade-offs, researchers from Carnegie Mellon's Department of Electrical and Computer Engineering and Washington State University identify a new approach for enabling energy-efficient multicore systems. Much like bypassing road congestion when traveling long distances, by using wireless on-chip communication between individually controllable clusters, researchers were able to

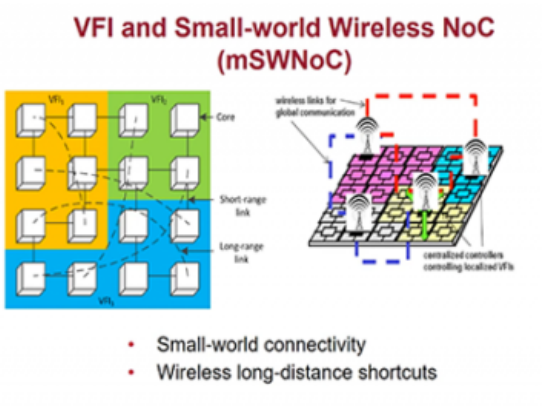
provide an efficient communication backbone, which can be tailored for large scale multicore systems. This paper presents a platform that is poised to save significant energy with little or no performance penalty. The article is the featured *IEEE Transactions on Computers* paper for the month of April.

As the number of cores packed into a single chip rises, scalable power management strategies are needed to keep power under prescribed limits. Voltage frequency islands, or VFIs, have long been used to enable such strategies. In VFI-based designs, the system is partitioned into islands with individually adjustable voltage and frequencies so as to reduce the power within allowable performance penalties.

However, while enabling significant power savings, a main challenge of VFI-based designs is the on-chip communication cost which negatively impacts application performance. Indeed, mixed voltage/frequency interfaces must be used for inter-VFI communication, thereby increasing communication delay.

This paper presents two innovative solutions, the first of which is through the VFI clustering methodology. A hybrid VFI clustering that combines both per-VFI utilization and inter-VFI communication enables minimal inter-VFI communication without greatly increasing the inter-cluster utilization variation. Secondly, researchers utilized a small-world wireless Network on Chip or mSWNoC to enable fast and energy efficient on-chip communication. The mSWNoC exploits small-world connectivity for reducing communication costs through wireless long-range short cuts between VFIs.





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The wireless small-world connectivity is able to mitigate most of the performance penalties introduced by VFIs. Furthermore, VFI-based multicore systems with mSWNoC communication are shown to be significantly better in energy efficiency compared to classic systems using wired on-chip networks (e.g. mSWNoC improves the energy dissipation by 40% and the energy-delay product by 52% compared to a wireline mesh on common PERSEC and SPLASH-2 benchmarks)

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