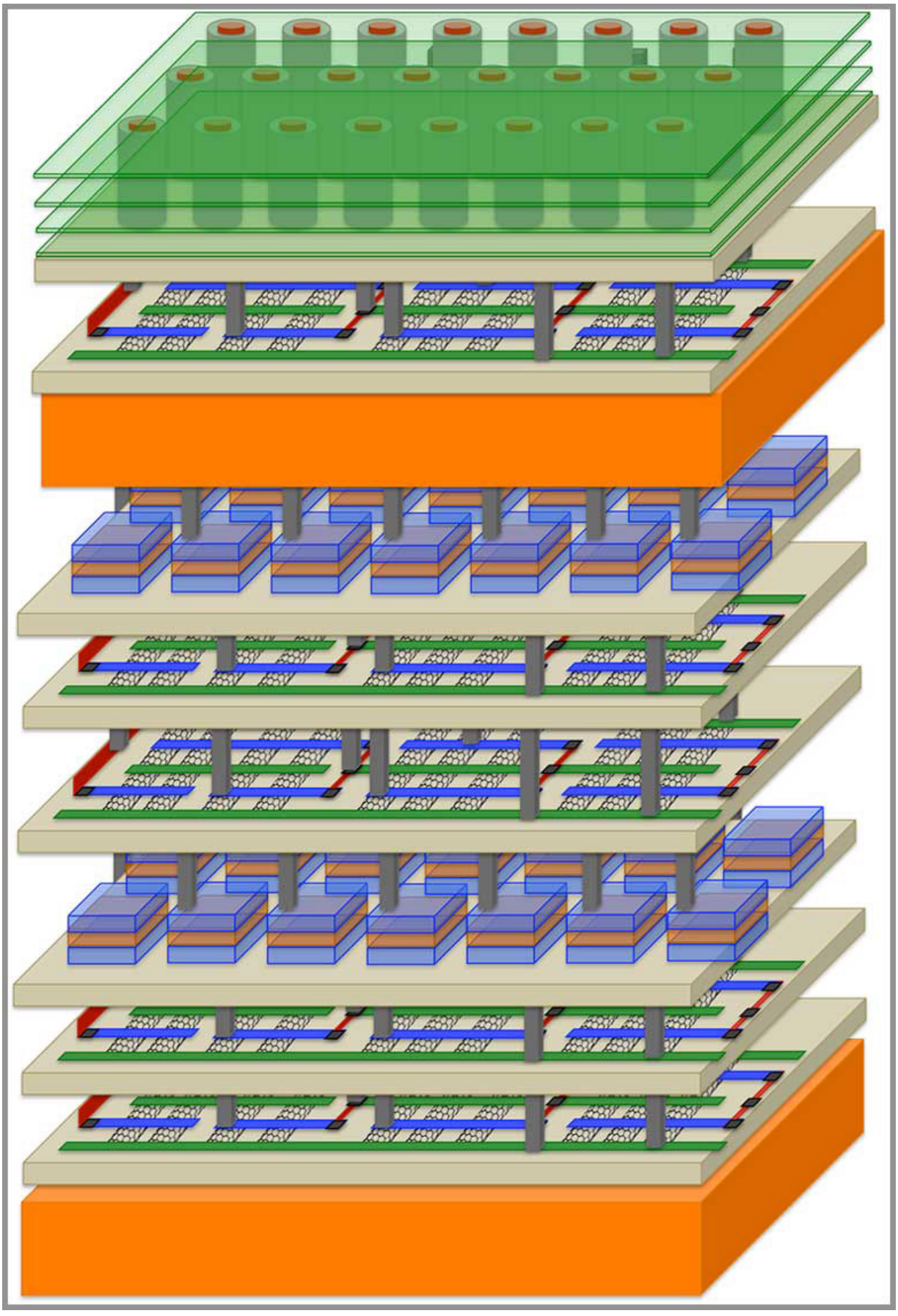
Skyscraper-style chip design boosts performance 1,000-fold

December 10 2015, by Ramin Skibba



A multi-campus team led by Stanford engineers Subhasish Mitra and H.-S. Philip Wong has developed a revolutionary high-rise architecture for computing.

For decades, engineers have designed computer systems with processors and memory chips laid out like single-story structures in a suburb. Wires connect these chips like streets, carrying digital traffic between the processors that compute data and the memory chips that store it.

But suburban-style layouts create long commutes and regular traffic jams in electronic circuits, wasting time and energy.

That is why researchers from three other universities are working with Stanford engineers, including Associate Professor Subhasish Mitra and Professor H.-S. Philip Wong, to create a revolutionary new high-rise architecture for computing.

In *Rebooting Computing*, a special issue of the *IEEE Computer* journal, the team describes its new approach as Nano-Engineered Computing Systems Technology, or N3XT.

N3XT will break data bottlenecks by integrating processors and memory like floors in a skyscraper and by connecting these components with millions of "vias," which play the role of tiny electronic elevators. The N3XT high-rise approach will move more data, much faster, using far less energy, than would be possible using low-rise circuits.

"We have assembled a group of top thinkers and advanced technologies to create a platform that can meet the computing demands of the future,"

Mitra said.

Shifting electronics from a low-rise to a high-rise architecture will demand huge investments from industry – and the promise of big payoffs for making the switch.

"When you combine higher speed with lower energy use, N3XT systems outperform conventional approaches by a factor of a thousand," Wong said.

To enable these advances, the N3XT team uses new nano-materials that allow its designs to do what can't be done with silicon – build high-rise computer circuits.

"With N3XT the whole is indeed greater than the sum of its parts," said co-author and Stanford electrical engineering Professor Kunle Olukotun, who is helping optimize how software and hardware interact.

New transistor and memory materials

Engineers have previously tried to stack silicon chips but with limited success, said Mohamed M. Sabry Aly, a postdoctoral research fellow at Stanford and first author of the paper.

Fabricating a silicon chip requires temperatures close to 1,800 degrees Fahrenheit, making it extremely challenging to build a silicon chip atop another without damaging the first layer. The current approach to what are called 3-D, or stacked, chips is to construct two silicon chips separately, then stack them and connect them with a few thousand wires.

But conventional, 3-D silicon chips are still prone to traffic jams and it takes a lot of energy to push data through what are a relatively few connecting wires.

The N3XT team is taking a radically different approach: building layers of processors and memory directly atop one another, connected by millions of electronic elevators that can move more data over shorter distances that traditional wire, using less energy. The N3XT approach is to immerse computation and memory storage into an electronic super-device.

The key is the use of non-silicon materials that can be fabricated at much lower temperatures than silicon, so that processors can be built on top of memory without the new layer damaging the layer below.

N3XT high-rise chips are based on carbon nanotube transistors (CNTs). Transistors are fundamental units of a computer processor, the tiny on-off switches that create digital zeroes and ones. CNTs are faster and more energy-efficient than silicon processors. Moreover, in the N3XT architecture, they can be fabricated and placed over and below other layers of memory.

Among the N3XT scholars working at this nexus of computation and memory are Christos Kozyrakis and Eric Pop of Stanford, Jeffrey Bokor and Jan Rabaey of the University of California, Berkeley, Igor Markov of the University of Michigan, and Franz Franchetti and Larry Pileggi of Carnegie Mellon University.

Team members also envision using data storage technologies that rely on materials other than silicon, which can be manufactured on top of CNTs, using low-temperature fabrication processes.

One such data storage technology is called resistive random-access memory, or RRAM. Resistance slows down electrons, creating a zero, while conductivity allows electrons to flow, creating a one. Tiny jolts of electricity switch RRAM memory cells between these two digital states. N3XT team members are also experimenting with a variety of nano-

scale magnetic materials to store digital ones and zeroes.

Just as skyscrapers have ventilation systems, N3XT high-rise chip designs incorporate thermal cooling layers. This work, led by Stanford mechanical engineers Kenneth Goodson and Mehdi Asheghi, ensures that the heat rising from the stacked layers of electronics does not degrade overall system performance.

Proof of principle

Mitra and Wong have already demonstrated a working prototype of a high-rise chip. At the International Electron Devices Meeting in December 2014 they unveiled a four-layered chip made up of two layers of RRAM memory sandwiched between two layers of CNTs.

In their N3XT paper they ran simulations showing how their high-rise approach was a thousand times more efficient in carrying out many important and highly demanding industrial software applications.

Stanford computer scientist and N3XT co-author Chris Ré, who recently won a "genius grant" from the John D. and Catherine T. MacArthur Foundation, said he joined the N3XT collaboration to make sure that computing doesn't enter what some call a "dark data" era.

"There are huge volumes of data that sit within our reach and are relevant to some of society's most pressing problems from health care to climate change, but we lack the computational horsepower to bring this data to light and use it," Re said. "As we all hope in the N3XT project, we may have to boost horsepower to solve some of these pressing challenges."

Provided by Stanford University