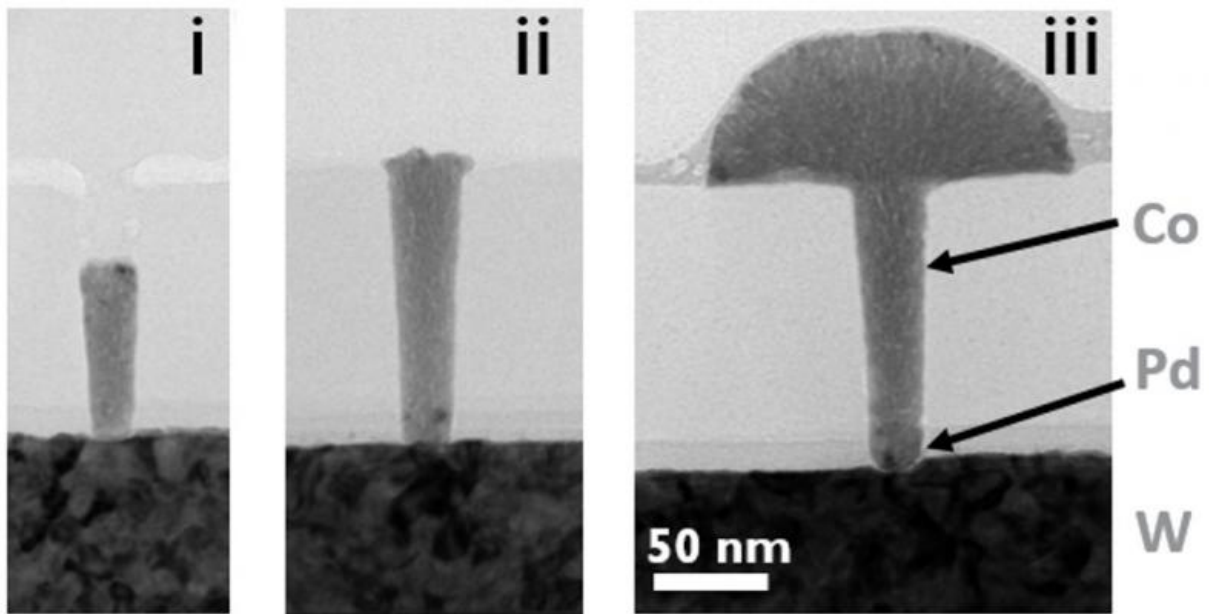


# Researchers develop novel metallization method

May 20 2015



Co ELD on Palladium/Tungsten (Pd/W) for different timed stops to yield an (i) under fill, (ii) potential ideal stop or an (iii) overburden in 28nm holes (Aspect Ratio (AR) 4.5).

During the IEEE IITC conference in Grenoble, the nanoelectronics research center imec and Lam Research Corporation today presented a novel bottom-up prefill technique for vias and contacts. The technique, based on Electroless Deposition (ELD) of Cobalt (Co) is a highly selective method resulting in void-free filling of via and contact holes.

Potentially increasing the circuit performance, it is a promising path to scaling advanced interconnects and enabling future logic and DRAM nodes at the 7 nm node and below.

As logic and memory nodes scale, performance of these advanced interconnects is negatively impacted by increasing interconnect resistance. Furthermore, voids that occur in heavily scaled vias severely impact yield. Imec's industrial affiliation program on advanced interconnects is exploring novel metallization methods to solve these issues. One way to solve the problem is to identify integration and metallization alternatives that provide resistance benefits over conventional technology without compromising reliability and yield.

Together with Lam Research, a Co ELD technique was demonstrated as a feasible method for highly selective bottom-up contact fill and via prefill with Cobalt (Co) as an alternative metal to Copper (Cu). Moreover, the high selectivity of the ELD process, at lower cost compared to Chemical Vapor Deposition (CVD), intrinsically ensures a good metal-to-metal interface and paves the way to void-free via filling and increased yield. Trench fill yield and line resistance may also benefit from the de-coupling of line and via aspect ratios, permitting the design of each for optimum Resistance/Capacitance (RC). Therefore, Co prefill ELD has the potential to enable future scaling of advanced logic and memory technologies.

Provided by IMEC

Citation: Researchers develop novel metallization method (2015, May 20) retrieved 25 April 2024 from <https://phys.org/news/2015-05-metallization-method.html>

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