Researchers demonstrate electrical advantages of direct CU etch scheme for advanced interconnects

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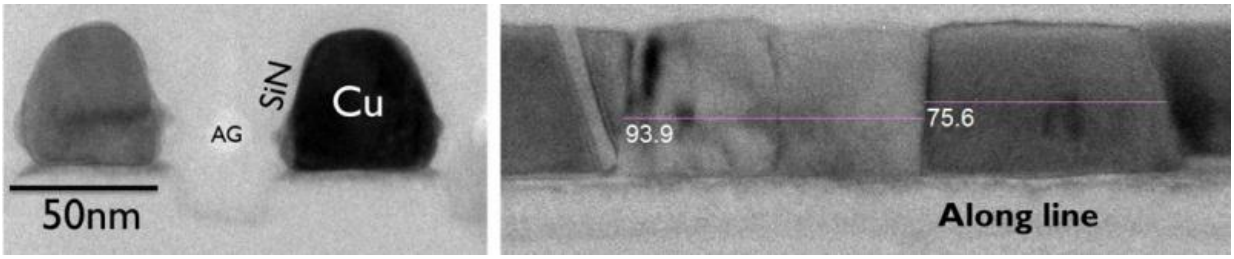

Figure TEM section of copper etched lines encapsulated by SiN cap layer.

Today, at the IEEE IITC conference, nano-electronics research center imec and Tokyo Electron Limited (TEL) presented a direct Cu etch scheme for patterning Cu interconnects. The new scheme has great potential to overcome resistivity and reliability issues that occur while scaling conventional Cu damascene interconnects for advanced nodes.

Aggressive scaling of damascene Cu interconnects leads to a drastic increase in the resistivity of the Cu wires, due to the fact that grain size is limited by the damascene trenches, which results in increased grain boundary and surface scattering. Additionally, the grain boundary negatively influences electromigration. When scaling damascene Cu interconnects, reliability issues occur because the overall copper volume

is reduced and interfaces become dominant. Imec and TEL have demonstrated the feasibility of a direct Cu etch scheme to replace the conventional Cu damascene process.

A key advantage of the direct Cu etch process is that it systematically results in larger grain sizes. Moreover, electromigration performance is preserved by applying an in-situ SiN cap layer that protects the Cu wires from oxidation and serves as the Cu interface.

Provided by IMEC