

Research reduces microprocessor serial link power consumption, improves data center energy efficiency

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University of Illinois at Urbana-Champaign researchers are working to reduce the serial link power consumption, thereby helping data centers and mobile platform operate more energy efficiently.

The University of Illinois research—sponsored by Semiconductor Research Corporation (SRC) through the Texas Analog Center of Excellence (TxACE)—was presented last month at the International Solid-State Circuits Conference (ISSCC).

Serial links consume about 20 percent of microprocessor power and constitute about 7 percent of overall energy consumption in a data center. These serial links are only sporadically used, such as when there is a request to access a webpage or a miss in the last level of cache.

"It is estimated that serial links are idle more than 50 to 70 percent of the time in many applications, but they still consume nearly all of link's power even in the idle state," said Pavan Kumar Hanumolu, an associate professor of Electrical and Computer Engineering at Illinois. "Our research seeks to reduce microprocessor serial link power consumption by eliminating the serial link idle power component completely."

As part of the research, the Illinois team designed a 7-gigabit per second transceiver with the first reported on/off embedded clock architecture. The new transceiver achieved an order of magnitude lower serial link



power-on compared to existing transceivers.

"The reduction of serial link power consumption not only benefits processors and mobile platforms, but it also reaps continued benefits from Moore's Law by increasing the computational capacity and offchip bandwidth for a few more years without adding pressure on the power envelop of the processor," said Hanumolu, who led the research team that also included Ph.D. student Tejasvi Anand.

Previous technology reports power-on lock times of a couple hundreds of nanoseconds for memory interfaces and a few microseconds in the case of Energy Efficient Ethernet (IEEE 802.3az). The long power-on lock time limits the opportunities of the serial link to save power. The Illinois research reduced the power-on lock time to less than 20 nanoseconds, and this resulted in a 44 times reduction in power.

The Illinois team began the research in 2011 and has reported on multiple advancements over the years, including presenting the new transceiver results at this year's ISSCC. The team estimates that data centers in North America can save \$870 million annually using this approach, with the yearly serial link power savings at <u>data centers</u> worldwide by 2020 equaling Japan's yearly electricity consumption.

"The conventional way to reduce power is to design and manufacture links on advanced nodes, which can be a costly proposition. The University of Illinois' approach achieves <u>power</u> savings that should be useful across many technology nodes, and that's one of the reasons this research is so compelling," said David Yeh, SRC director of Integrated Circuits and Systems Sciences.

The Illinois transceiver technology can be implemented on any technology node from a manufacturing standpoint, with the research results being demonstrated on 90 and 65 nanometer nodes. The



technology can also apply to memory and networking applications.

More information: "3.7 A 7Gb/s rapid on/off embedded-clock seriallink transceiver with 20ns power-on time, 740µW off-state power for energy-proportional links in 65nm CMOS." <u>DOI:</u> <u>10.1109/ISSCC.2015.7062927</u>

Provided by Semiconductor Research Corporation

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