

HiSIM-SOTB, compact transistor model, selected as international industry standard

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A new compact transistor model was developed and the framework for realizing a faster design support process and product development for integrated circuits in the ultra-low voltage category was established. The new compact model, HiSIM-SOTB (Hiroshima University STARC IGFET Model Silicon-on-Thin BOX), was developed by Hiroshima University's HiSIM Research Center in collaboration with its partners in the industry and government institutions, including the National Institute of Advanced Industrial Science and Technology (AIST) of Japan. On June 20, 2014, after a two-year-long effort by the industry/government/academia research team, this new model was selected as an international industry standard during a meeting in Washington D.C., which was held by the Compact Modeling Coalition (CMC) of the Silicon Integration Initiative (Si2).

Following this selection, Hiroshima University made HiSIM-SOTB open to the public through its HiSIM Research Center's website (<http://www.hisim.hiroshima-u.ac.jp/index.php?id=87>) on January 9, 2015.

HiSIM-SOTB accurately replicates the characteristics of the SOTB-MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor), which is expected to become a practical transistor structure for super-low-power-consumption by lowering the operating voltage of [integrated circuits](#). The research team, which was led by Prof. Mitiko Miura-Mattausch, HiSIM Research Center of Hiroshima University (headed by Prof. Hans Jurgen Mattausch) and Dr. Hanpei Koike, Leader,

Electroinformatics Group, Nanoelectronics Research Institute (headed by Dr. Tetsuji Yasuda) of AIST, successfully implemented the loop between Hiroshima University's development of the transistor model and AIST's reproduction tests of measured data. The results verify that HiSIM-SOTB enables the accurate simulation of circuit operations in the case of substantially lowered supply voltages for transistor operation, ranging from 1 V to 0.4 V.

By solving the Poisson equation, HiSIM-SOTB accurately finds the surface potentials at three required positions: the upper and lower sides of the ultrathin SOI (Silicon-on-insulator as a silicon channel layer) film, and the upper side of the substrate. For this purpose, the device physics was represented using three basic equations. To solve these equations including the three surface potentials, it was necessary to address the challenge of stably solving the third-order Newton equation in order to obtain their numerical solutions. However, by developing an appropriate algorithm, the research group has enabled HiSIM-SOTB to accurately reproduce the changes in the substrate-carrier concentration and in the carrier distribution as a function of the applied substrate bias voltage. In parallel, HiSIM-SOTB includes a variety of ingenious twists to shorten the calculation time. HiSIM-SOTB has subsequently been completed as an ultimate compact model that is applicable to any device structure.

During the early stages of the development of HiSIM-SOTB, the cooperation that leveraged the strengths of each of our partners in industry, government, and academia was beneficial. This collaboration was carried out based on each partner's previous attempts to realize a standardized compact transistor model. The realization of this effective and rapid cooperation was one of the major reasons why the research team could solve the problems related to the perfection of a compact model for the standardization within the limited time available. Indeed, this collaboration has enabled the ideal scenario to be realized, in that before finalizing the device's design, the evaluation of the circuit

characteristics was completed, and an environment for large-scale circuit design was already established.

Provided by Hiroshima University

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