Renesas announces SRAM using leading-edge 16 nm FinFET for automotive information systems

December 19 2014

Renesas Electronics today announced the development of a new circuit technology for automotive information SoCs (system on chips) at 16 nanometer (nm) and beyond. Using this new circuit technology, Renesas tested the prototype of an SRAM, at the 16 nm node as the cache memory for CPU and real-time image processing blocks in an SoC, and successfully confirmed that this SRAM operates at the high speed of 641 ps under the low-voltage condition of 0.7 V.

Recently, automotive information systems, such as car navigation systems and advanced driver assistance systems (ADAS), are designed with the automatic driving systems of the future in mind, and have seen significant evolution. As a result, there are now strong demands for increased performance in aspects such as lower voltage operation and higher operating speeds in the CPU and real-time image processing, and the planar MOSFET devices used up to now are said to have reached their limits.

To address these demands, the new FinFET adopts a finned structure, to suppress power consumption and increase performance. It is, however, difficult to optimize the circuit constants in these FinFETs, and the development of new circuit design technologies has become an issue.

To overcome this issue, Renesas has now developed a new circuit technology for FinFET devices to allow high-speed read and write

operations to be performed in a stable manner even at low operating voltages.

Key features of the newly-developed circuit technology:

(1) The word line overdrive method makes both high-speed read/write operations possible at low voltages

Due to the increasing variations in device elements associated with decreasing feature sizes in semiconductor processes, there is a tendency for the device's lower-limit operating voltage characteristic to be degraded. Renesas has introduced a circuit technology (referred to below as an assist circuit) that works around this problem at the circuit level. Previously, to assure stable operation during the readout operations, the word line voltage was lowered slightly during memory access. However, this results in degraded margins during write operations and makes readout significantly slower. Renesas has now taken advantage of the characteristics of the FinFET device and, inversely to what was previously done, increases the word line voltage slightly; adopting the so-called assist circuit method, which changes those pulse widths during read and write. This technique assures adequate margins during read/write operations and thus achieves high-speed read operations in these devices.

(2) High-reliability optimal designs that take the variations inherent in the FinFET device into account

Unlike the earlier planar MOSFET, this new FinFET device has significant device to device variations. Due to the fact that an offset is generated in the currents that flow on the bit lines during readout between the center and edge sections of memory cells arranged in an array, current differences occur and it becomes no longer possible to

assure adequate sense amplifier margins. As a result, devices may not function correctly. Therefore it is necessary to design for margins that are adequate for these current differences. Now, Renesas has quantitatively verified this current offset by measurement in a prototype chip. These actual measurements made it possible to perform fine adjustment of the circuit so that optimal operating margins can be assured. This technique will contribute to achieving the high reliability desired in devices for automotive information equipment as feature sizes continue to shrink.

The newly-developed assist circuit technology makes it possible to achieve both high speed and stable operation, which are expected to be problematic as device fabrication process feature sizes continue to shrink, and it will contribute significantly to performance improvements in real-time image processing that is required for the leading-edge driving support systems and automated driving systems of the future.

Renesas intends to contribute to the creation of a safe, secure, and pleasurable driving experience by adopting this newly-developed SRAM in Renesas' leading-edge SoC products using the 16 nm FinFET fabrication process and quickly providing these products to our customers.

Provided by Renesas Electronics